

Modeling and Simulation of Interline Dynamic Voltage Restorer for Voltage Sag/Swell Compensation

Usha Rani P.

Assosiate Prof, E.E.E Department,
Jerusalem College of Engineering,
Chennai, India.
pusharani71@yahoo.com

Sudha R., Rajkumar.M

PG Scholar, Power Electronics and Drives,
Jerusalem College of Engineering,
Chennai, India.

Dr. S. Rama Reddy

Professor, E.E.E. Department,
Jerusalem College of Engineering,
Chennai, India.
srr_victory@yahoo.com

Abstract— The Dynamic Voltage Restorer (DVR) provides an advanced and economical solution for both voltage sag and swell problems. The voltage-restoration process involves real-power injection into the distribution system. The Interline DVR (IDVR) proposed in this paper provides a way to compensate the voltage deviation caused in a feeder. The IDVR consists of several DVRs connected to different distribution feeders in the power system sharing a common energy storage. Here, one DVR in the IDVR system works in voltage-sag/swell compensation mode while the other DVR in the IDVR system operate in power-flow control mode. The single phase model of the IDVR system is illustrated which is operated by Multiple Pulse Width Modulation (PWM). Open-loop and closed-loop control schemes of load voltage for a simple system is modeled and simulated using MATLAB software. The simulation results are presented to demonstrate the effectiveness of the proposed IDVR system.

Keywords— Interline Power Flow Controller (IPFC), Multiple Pulse width modulation(PWM), power flow control mode, series compensation, Total Harmonic Distortion(THD)

I. INTRODUCTION

The need of the electrical power is increasing and simultaneously the problems while transmitting the power through the distribution system are also increasing. Voltage fluctuations are considered as one of the most severe power quality disturbances to be dealt with. Even a short-duration voltage fluctuation could cause a malfunction or a failure of a continuous process. There are several types of voltage fluctuations that can cause the systems to malfunction, including surges and spikes, sag, swell, harmonic distortions, and momentary disruptions. Among them, voltage sag and swell are the major power-quality problems.

Voltage sag is the sudden decrease of the voltage to about 10-90% of the supply voltage. This is caused due to the sudden increase of load across that particular feeder. Whereas, voltage swell is the sudden increase of voltage to about more than 110% amplitude of the supply voltage. This is caused due to the sudden reduction of the load across that particular feeder. This increase or decrease of voltage is compensated by injecting the voltage in series with the supply from another feeder at the time of disturbances using DVR. This IDVR system is presently one of the most cost-effective and a highly efficient method to mitigate voltage sag or swell.

The concept of Interline Dynamic Voltage Restorer (IDVR) where two or more voltage restorers are connected such that they share a common DC-link is similar to the

Interline Power Flow Controller (IPFC) concept. In this paper, a two-line IDVR system is explained which employs two DVRs connected to two different feeders originating from two grid substations, could be of the same or different voltage level. However the DC-link of these two DVRs could be connected to a common DC-link. This would cut down the cost as sharing a common DC-link reduces the DC-link storage capacity significantly compared to that of a system whose loads are protected by clusters of DVRs with separate energy storages. When one of the DVRs compensates for voltage sag or swell produced, the other DVR in IDVR system operates in power-flow control mode. This is to replenish DC-link energy storage, which is depleted due to the power taken by the DVR working in the voltage-sag/swell compensation mode. The DVR is operated in such a fashion that it does not supply or absorb any active power during the steady-state operation [1]. It is desirable to have a minimum VA rating of the DVR, for a given system without compromising compensation capability [2]. Control algorithm for dynamic voltage restorer (DVR) to improve voltage quality problems such as voltage sags/swells in distribution systems has been proposed [3]. The DVR consists of three inverters sharing the same DC link via a capacitor bank. Each inverter has an individual inner control loop for generating the gate signals for the switches [4]. The lines in the IPFC originate from a single grid substation while the lines in the IDVR system originate from different grid substations. The voltage-restoration process involves real-power injection into the distribution system, the capability of a particular DVR topology, especially for compensating long-duration voltage sags, depends on the energy storage capacity of the DVR [5]. The main factors which limits capabilities of a particular DVR in compensating long-duration voltage sags is the amount of stored energy within the restorer [6]. The modeling and simulation of Z source impedance based DVR is presented in [8]. The closed loop control modeling simulation of IDVR is presented [7].

II. PRINCIPLES OF OPERATION OF IDVR

The IDVR system consists of several DVRs in different feeders, sharing a common DC-link. A two-line IDVR system shown in Figure 1 employs two DVRs are connected to two different feeders where one of the DVRs compensates for voltage sag or swell produced, the other DVR in IDVR system operates in power-flow control mode.

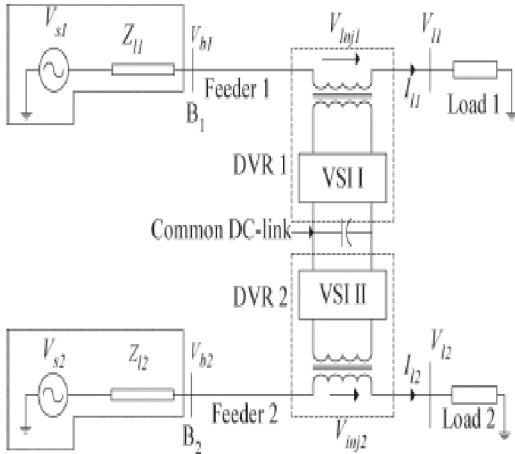


Figure 1 Schematic diagram of an IDVR in a two feeder system

Voltage sag/swell in a transmission system are likely to propagate to larger electrical distance than that in a distribution system. Due to these factors, the two feeders of the IDVR system in Figure 1 are considered to be connected to two different grid substations. It is assumed that the voltage distortion in Feeder₁ would have a lesser impact on Feeder₂.

A. Elements of an IDVR System

The upstream generation-transmission system is applied and the two feeders can be considered as two independent sources. These two voltage sources V_{s1} and V_{s2} are connected in series with the line impedances Z_{l1} and Z_{l2} which is in-turn connected to the buses B_1 and B_2 as in Figure 1. The DVR is connected in series with the feeder and the DVRs across different feeders are connected by a common DC-link. The common DC-link indicated between the two DVRs is a large capacitor that acts as a voltage storage device. A Voltage Source Inverter (VSI) is present to invert the DC supply to AC voltage, which is injected to the transformer. The load across each feeder is connected in series to the DVR, where V_{l1} and V_{l2} are the voltages across the load.

B. Energy Storage Requirement of an IDVR System

The injection of an appropriate voltage needs a certain amount of real and reactive power which must be supplied by the DVR. Supply of real power is met by means of an energy storage facility connected in the DC-link. Large capacitors are used as a source of energy storage in most of the DVRs. Generally, capacitors are used to generate reactive power in an AC power system. However, in a DC system, capacitors can be used to store energy. When the energy is drawn from the energy storage capacitors, the capacitor terminal voltage decreases. Hence, large capacitors in the DC-link energy storage are needed to effectively mitigate voltage sag/swell of large depths and long durations.

C. Modulation Technique for Pulse Generation

The pulse can be generated using various modulation techniques. In this paper, the pulse for the switch is generated using Multiple Pulse Width Modulation (PWM).

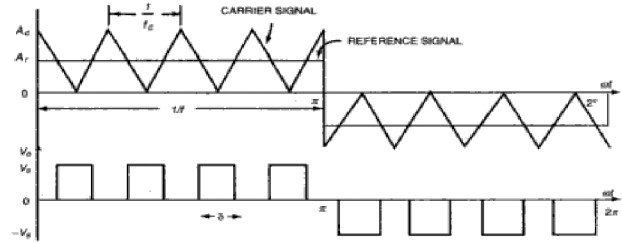


Figure 2 Multiple Pulse Width Modulation

The output of the rectifier that converts the AC output voltage from the DVR₁ to a DC voltage is further controlled by Pulse Width Modulation (PWM), which is generated by comparing a triangular wave signal with an adjustable DC voltage supplied from DVR₂ of Feeder₂. Hence the duty cycle of the switching pulse could be varied to synthesis the required conversion. This stream of PWM is shown in Figure 2.

III. VOLTAGE SAG COMPENSATION IN A TWO FEEDER IDVR SYSTEM

The voltage sag in a two-feeder IDVR system is caused due to sudden increase of the load across a feeder. Consider the condition when the DVR₁ in the IDVR system operates in voltage-sag compensating mode while the DVR₂ operates in power-flow control mode to keep the DC-link voltage at a desired level. When there is no voltage disturbance, the load voltage of Feeder₂ is equal to the bus voltage V_{b2} . During voltage sag, the DVR₂ should be operated to meet this condition while supplying real power to the common DC-link. The two control schemes, open loop and closed loop, are illustrated.

A. Open loop control of voltage sag compensation in an IDVR system

The simulink model of the open loop controlled IDVR for voltage sag compensation is shown in Figure 3. The two feeders, each consisting of DVR connected in series to the line are connected to each other by a common DC-link. For an open loop control, separate pulse is given to the rectifier. The rectifier converts the AC voltage from Transformer₂ of Feeder₂ to DC voltage which is inverted back to AC and given to the Transformer₁ of Feeder₁.

Consider the system has been subjected to sudden increase of load across Feeder₁ leading to voltage sag at, say, $t=300\text{ms}$ and it remains till the load is reduced back to the original state, say until $t=700\text{ms}$ with a total voltage sag duration of 400ms. At that particular point of time, the voltage is injected in-phase from the healthy Feeder₂. This voltage undergoes rectification

and inversion to reduce the harmonics. The AC voltage from Feeder₂ is converted to DC voltage and then back to AC voltage which is fed to Feeder₁. Here, the Multiple Pulse Width Modulation (PWM) technique is used to create pulses, which is given to both the rectifier and inverter. Filters are added to reduce harmonics. The capacitance present between the rectifier and the inverter acts as a common DC-link source.

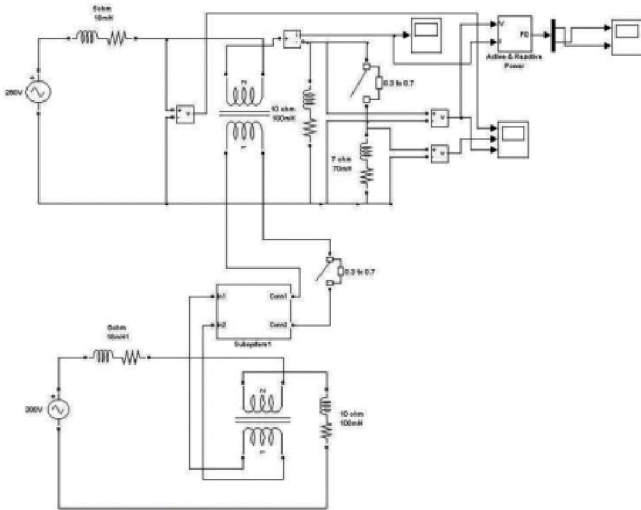


Figure 3 Open loop control of voltage sag compensation

The Figure 4 shows the response of voltage sag compensation in an open loop control of two feeder IDVR system. The 260V input voltage is subjected to a sag of 20% magnitude. The voltage is injected from Feeder₂ and as a result the load voltage is maintained at the same value throughout, including the voltage sag period. The voltage-sag compensation involves injection of real and reactive power to the distribution system, and this determines the capacity of the energy storage device required in the restoration scheme. The reactive power requirement can be generated electronically within the voltage source inverter of the DVR. Thus, the maximum amount of real power that can be supplied to the load during voltage-sag compensation is a deciding factor of the capability of a DVR, especially for mitigating long-duration voltage sags.

The real and reactive power across the Feeder₁ is presented in Figure 5. At the point of voltage injection, both the real and reactive power is increased. This increase in the power indicates the compensation of the voltage level in the feeder. The line spectrum for the compensated voltage is taken to determine the Total Harmonic Distortion present in the waveform. The Figure 6 shows the Total Harmonic Distortion (THD) is 2.83% for a 20% of voltage sag.

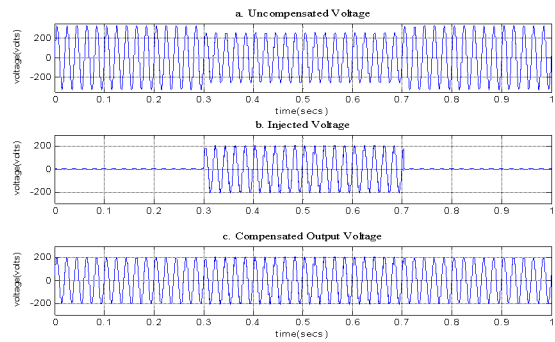


Figure 4 Simulated results of Open loop IDVR at 20% Voltage Sag
a. Uncompensated voltage
b. Injected voltage
c. Compensated output voltage

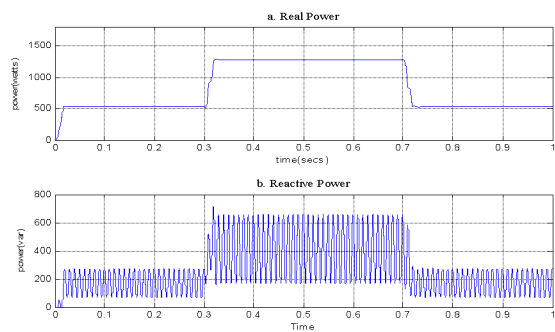


Figure 5 Real and reactive powers of feeder₁ in open loop control of voltage sag compensation in IDVR system
a. Real power
b. Reactive power

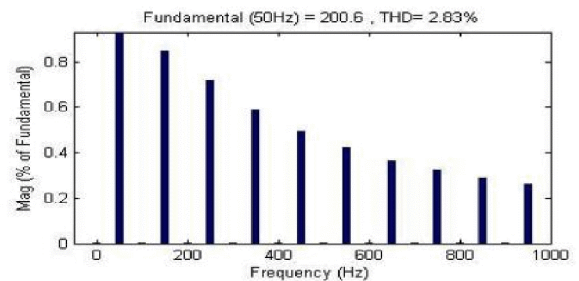


Figure 6 FFT analysis of output voltage sag waveform of open loop control

B. Closed loop control of voltage sag compensation in an IDVR system

The simulink model of the closed loop controlled IDVR for voltage sag compensation is shown in Figure7. For a closed loop control, the output voltage from the load across the load is rectified to give a DC voltage. This DC voltage is controlled via PI controller. The error is used and the driving pulse is generated. This pulse is fed to the rectifier which therefore yields in the injection of voltage. The injected voltage of the DVR depends on the accuracy and dynamic behavior of the pulsewidth-modulation.

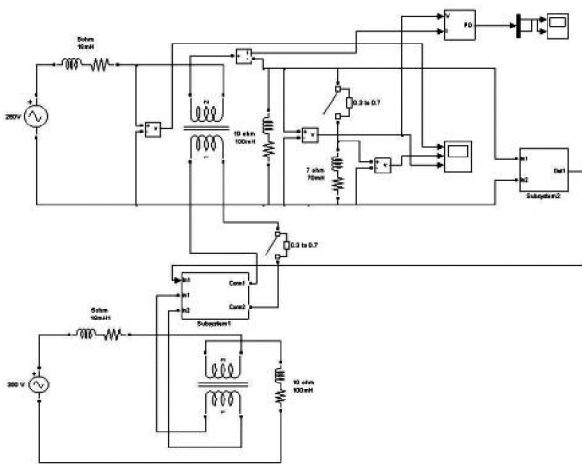


Figure 7 Closed loop control of voltage sag compensation

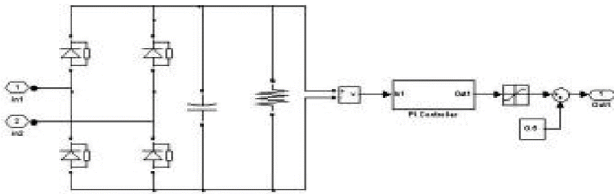


Figure 8 Subsystem for voltage sensing and comparison for closed loop control of voltage sag compensation

The Figure 8 shows the rectification of the output voltage. Here the AC voltage is converted to DC voltage and controlled by a PI controller. The error is used to generate the driving pulse. The general requirement of such control scheme is to obtain an AC waveform with low Total Harmonic Distortion (THD) and good dynamic response against supply and load disturbance whether the DVR in the IDVR system operates in voltage sag compensation or power flow control mode.

The Figure 9 shows the response of voltage sag compensation in a closed loop control of a two feeder IDVR system. The 260V input voltage is subjected to a sag of 20% magnitude. The voltage is injected from Feeder₂ and as a result the voltage is maintained at the same value throughout the simulation, including the voltage sag period. Figure 10 shows the real and reactive power obtained across Feeder₁. Both the real and reactive power is increased when there is an increase in the load. Compared to that of the open loop control, the real and reactive power in a closed loop control is greater with comparatively less disturbances.

The line spectrum for the compensated voltage is taken to determine the Total Harmonic Distortion (THD) present in the waveform. The Figure 11 shows the Total Harmonic Distortion (THD) is 2.39% for a 20% of voltage sag. The distortions produced in the voltage waveform for a closed loop control is comparatively lesser than that of the open loop control. Hence closed loop has greater efficiency compared to the open loop control scheme.

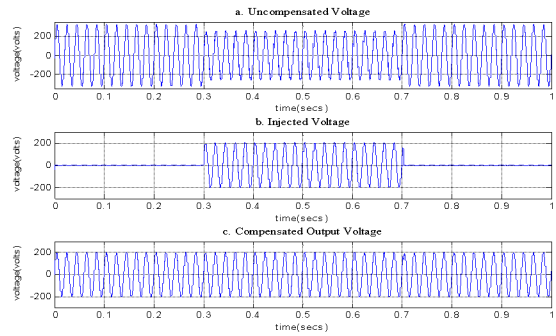


Figure 9 Simulated results of closed loop IDVR at 20% voltage sag
a. Uncompensated voltage
b. Injected Voltage
c. Compensated output voltage

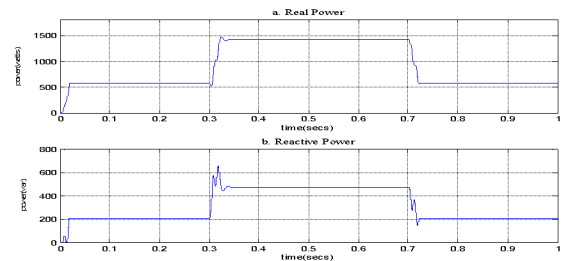


Figure 10 Real and reactive powers of feeder₁ in closed loop control of voltage sag compensation in IDVR system
a. Real power
b. Reactive power

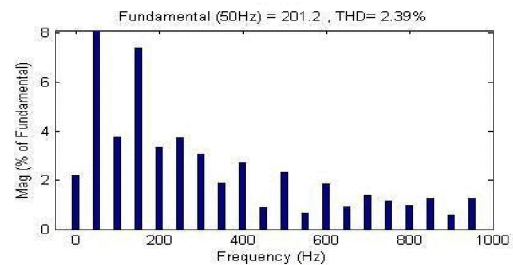


Figure 11 FFT analysis of output voltage sag waveform of closed loop control

IV. VOLTAGE SWELL COMPENSATION IN A TWO FEEDER IDVR SYSTEM

The voltage swell in a two-feeder IDVR system is caused due to sudden decrease of the load across a feeder. Consider the condition when the DVR₁ in the IDVR system operates in voltage-swell compensating mode while the DVR₂ operates in power-flow control mode to keep the DC-link voltage at a desired level. When there is no voltage disturbance, the load voltage of Feeder₂ is equal to the bus voltage V_{b2} . During voltage swell, the DVR₂ should be operated to meet this condition while supplying real power to the common DC link. The two control schemes, open loop and closed loop, are illustrated.

A. Open loop control of voltage swell compensation in an IDVR system

The simulink model of the open loop controlled IDVR for voltage swell compensation is shown in Figure 3. Consider the system has been subjected to sudden decrease of load across Feeder₁ leading to voltage swell at, say, t=300ms and it remains till the load is reduced back to the original state, say until t=700ms with a total voltage swell duration of 400ms. At that particular point of time, the voltage is injected out-of-phase from the healthy Feeder₂.

The Figure 12 shows the response of voltage swell compensation in an open loop control of two feeder IDVR system. The 260V input voltage is subjected to swell of 20% magnitude. The voltage is injected from Feeder₂ and as a result the load voltage is maintained at the same value throughout, including the voltage swell period.

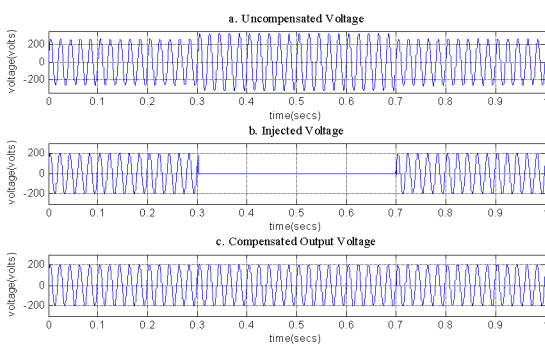


Figure 12 Simulated results of open loop IDVR at 20% voltage swell
 a. Uncompensated voltage
 b. Injected voltage
 c. Compensated output voltage

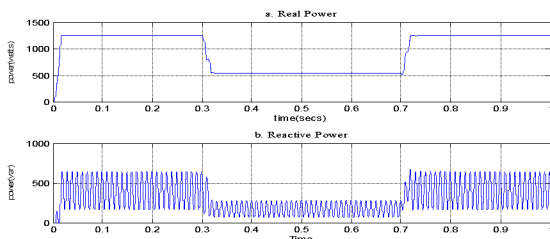


Figure 13 Real and reactive powers of feeder₁ in open loop control of voltage swell compensation in IDVR system
 a. Real power
 b. Reactive power

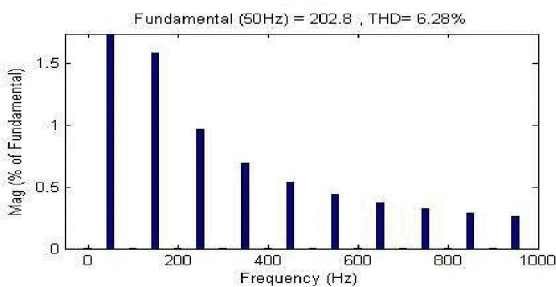


Figure 14 FFT analysis of output voltage swell waveform of open loop control

The real and reactive powers across the Feeder₁ are presented in Figure 13. At the point of voltage injection, both the real and reactive power is decreased. This decrease in the power indicates the compensation of the voltage level in the feeder. The line spectrum for the compensated voltage is taken to determine the Total Harmonic Distortion (THD) present in the waveform. The Figure 14 shows the Total Harmonic Distortion is 6.28% for a 20% of voltage swell.

B. Closed loop control of voltage swell compensation in an IDVR system

The simulink model of the closed loop controlled IDVR for voltage swell compensation is shown in Figure 7. For a closed loop control, the output voltage from the load across the load is rectified to give a DC voltage. This DC voltage is controlled via PI controller. The error is used and the driving pulse is generated. This pulse is fed to the rectifier which therefore yields in the injection of voltage.

The Figure 15 shows the response of voltage swell compensation in a closed loop control of two feeder IDVR system. The 260V input voltage is subjected to a swell of 20% magnitude. The voltage is injected out-of-phase from feeder₂ and as a result the load voltage is maintained at the same value throughout the simulation, including the voltage swell period. Figure 16 shows the real and reactive power obtained across feeder₁. Both the real and reactive power is decreased when there is an decrease in the load. Compared to that of the open loop control, the real and reactive power in a closed loop control is greater with comparatively less disturbances.

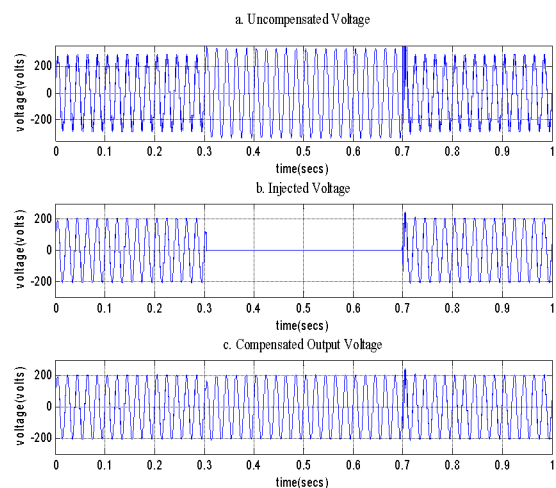


Figure 15 Simulated results of closed loop IDVR at 20% voltage swell
 a. Uncompensated voltage
 b. Injected voltage
 c. Compensated output voltage

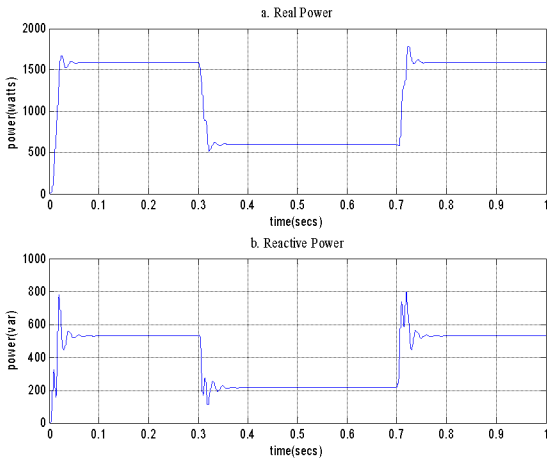


Figure 16 Real and reactive powers of feeder₁ in closed loop control of voltage swell compensation in IDVR system
 a. Real power
 b. Reactive power

The line spectrum for the compensated voltage is taken to determine the Total Harmonic Distortion (THD) present in the waveform. The Figure 17 shows the Total Harmonic Distortion (THD) is 5.27% for a 20% of voltage swell. The distortions produced in the voltage waveform for a closed loop control is comparatively lesser than that of the open loop control. Hence closed loop has greater efficiency compared to the open loop control scheme.

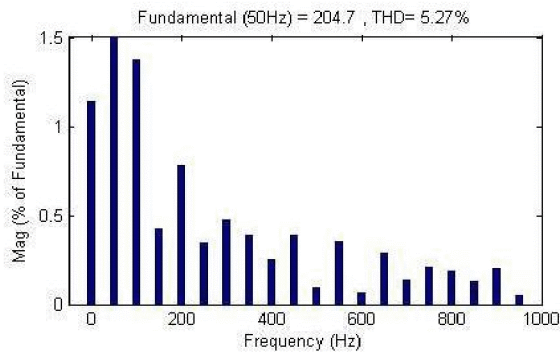


Figure 17 FFT analysis of output voltage swell waveform of closed loop control

The DC links of the DVRs can be connected to a common terminal, thereby forming an IDVR system. This would cut down the cost of the custom power device, as sharing common DC link reduces the size of the DC link storage capability substantially, compared to that of a system in which loads are protected by clusters of DVRs with separate energy storage systems. The cost of DC link for IDVR is half of the cost of two DVRs with separate DC link. Efficiency will not change. However, regulation of Feeder₁ would be better after the compensation.

V. CONCLUSION

Hence the simulink model for 20% of voltage sag and swell compensation in both the control schemes has been modelled and simulated. The respective THD values are obtained is shown.

Voltage Sag Compensation

Open loop control	2.83
Closed loop control	2.39

Voltage Swell Compensation

Open loop control	6.28
Closed loop control	5.27

The harmonics are comparatively lower for closed loop control scheme than in open loop control. The voltage compensation for both sag and swell can be implemented in a three phase IDVR system for various types of modulations.

REFERENCES

- [1] Arindam Ghosh, Amit Kumar Jindal, and Avinash Joshi,(2004) 'Design of a Capacitor-Supported Dynamic Voltage Restorer (DVR) for Unbalanced and Distorted loads' IEEE transactions on power delivery, vol. 19, no. 1.J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.
- [2] Anil Kumar. R, Siva Kumar. G (2009) 'Compensation of Voltage Sags and Harmonics with Phase-Jumps through DVR with minimum VA rating Using Particle Swarm Optimization' pp. 1361
- [3] Boonchiam. P, and Mithulananthan.N (2006) 'Dynamic Control Strategy in Medium Voltage DVR for Mitigating Voltage Sags/Swells' International Conference on Power System Technology.
- [4] Carl Ngai-Man Ho (2010) 'Implementation and Performance Evaluation of a Fast Dynamic Control Scheme for Capacitor-Supported Interline DVR', IEEE transactions on power electronics, vol. 25, no. 8.
- [5] Mahinda Vilathgamuwa.D (2006) 'A Novel Technique to Compensate Voltage Sags in Multiline Distribution System—The Interline Dynamic Voltage Restorer' IEEE transactions on industrial electronics, vol. 53, no. 5.
- [6] Mahinda Vilathgamuwa. D (2004) 'Interline Dynamic Voltage Restorer: A Novel and Economical Approach for Multiline Power Quality Compensation', IEEE transactions on industry applications, vol. 40, no. 6.
- [7] Usha Ran.P, Sudha..R, S.Rama reddy (2011),” Voltage sag/ swell compensation in an Interline Dynamic Voltage Restorer”, International conference on emerging trends in electrical and computer technology, IEEE Xplorer (978-1-4244-7925-2/11 IEEE), pp.309-314.
- [8] Usha Ran.P, Sudha..R, S.Rama reddy (2011),” Voltage sag/ swell compensation using Z source inverter based Dynamic Voltage Restorer”, International conference on emerging trends in electrical and computer technology, IEEE Xplorer (978-1-4244-7925-2/11 IEEE), pp.268-273.



P. Usha Rani is Associate professor in Electrical and Electronics Engineering Department, Jerusalem College of Engineering, Chennai, India. She received her B.E. degree in Electrical & Electronics Engineering from the Government College of Technology, Coimbatore, India in 1991, M.E. degree

in Power Systems from College of Engineering, Anna University, Chennai, India in 2001. Her earlier industrial experience of 5 years was with Chemin Controls, Pondicherry, India. She has 14 years of teaching experience. Her research interests include FACTS and application of power electronics to power quality problems.

published over 20 technical papers in national and international conferences proceedings / journals. He has secured the A.M.I.E. institution gold medal for obtaining the highest marks. He has secured the AIMO best project award. He has worked with Tata Consulting Engineers, Bangalore and Anna



S. Rama Reddy is Professor and Dean of Electrical & Electronics Engineering Department, Jerusalem College of Engineering, Chennai, India. He obtained his D.E.E. from S.M.V.M. polytechnic, Tanuku, A.P., A.M.I.E. in Electrical Engineering

from Institution of Engineers (India), M.E. in Power Systems from Anna University, Chennai and Ph.D in the area of Power Electronics from Anna University, Chennai, India. He has