ANALYSIS OF NEW REDUCED COUNT SINGLE PHASE MULTILEVEL INVERTER

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Abstract— *The paper brings out a new topology for a single phase multilevel inverter (MLI) in an effort to reduce the number of switches in the path for the flow of current. The emphasis encompasses flexibility on the number of levels of the output voltage in accordance with the specific requirements at the utility end. The second perspective owes to equalize the number of switching to synthesize each output level in addition to enabling a reduction in the total harmonic distortion (THD) of the output voltage. The variation in the carrier wave frequency allows the sinusoidal reference to mitigate the higher frequency components of the output voltage and contribute to an increase in its fundamental component. The MATLAB based simulation results enliven the ability of the variable frequency carrier band (VFCB) pulse width modulation (PWM) strategy to obviate the performance of the multicarrier PWM in terms of an improved spectrum for the output voltage. The experimental reading obtained through the use of field programmable gate array (FPGA) validates the simulated response and claims its viability for use in real world applications.*

Key Words- *Multilevel inverter**,** Variable frequency carrier band pulse width modulation, Field programmable gate array, Total harmonic distortion, Phase disposition.*

1. INTRODUCTION

The advent of multilevel inverters (MLIs) allows exploring a fresh scope for addressing the challenges in high voltage and high power applications. Besides the MLIs forge a renewed attention in light of the emergence of high power devices and innovative control techniques [1-3]. The use of MLI appears to experience an increasing trend in light of the extensive automation prevalent in industries.

The general function of the MLI engages to synthesize a desired high voltage from several levels of dc voltages that can be batteries, fuel cells among others [4-6]. It appears to be a suitable alternative for two level inverters in medium/high power applications due to reduced voltage distortion, lesser voltage stress, lower electromagnetic interference (EMI) and transfer of improved quality of power.

The cascade inverter, neutral-point clamped (NPC) inverter and flying capacitor (FC) inverter constitute the basic varieties of MLI topologies. With increase in the output level, while the NPC requires larger number of clamping diodes, the number of storage capacitors increase in the flying capacitor. Despite the fact that the classical MLI structures continue to support the application requirements, still the device count becomes significantly high with the increase in the number of voltage levels [7-8].

Single phase cascaded MLI has been proposed and a multicarrier scheme employed to generate the gating signals in the power switches [9]. The simulation results have been verified using an experimental prototype and the THD values validated.

A novel cascaded MLI topology has been suggested and the symmetric operation of the converter discussed. The number of switch count and the gate drivers has been reduced compared to cascaded H-bridge converter [10]. The simulation and experimental results have been presented and the effectiveness of the MLI structure brought out.

A symmetric MLI suitable for the medium voltage and higher number of output levels has been introduced [11]. The topology has been developed to generate the range of output levels with lower number of circuit devices that includes switches and gate drivers.

A single phase cascaded MLI has been explained to comprise of a series connection of a basic unit and with a facility to add a H-bridge to [12].The inverter has been able to

generate both odd and even voltage levels and the results validated using hardware prototype.

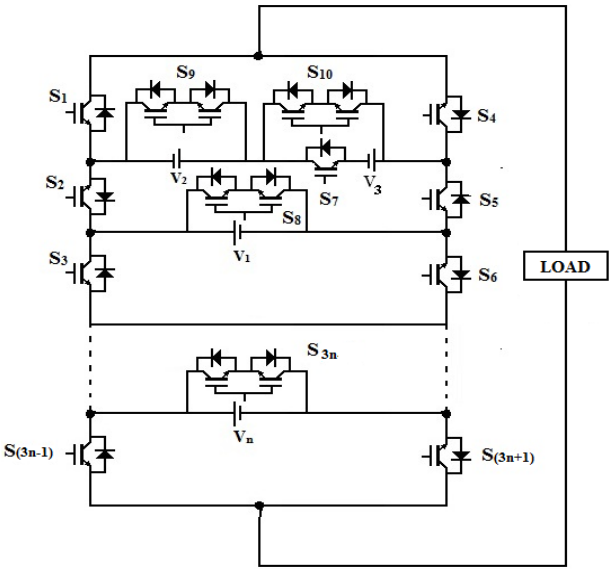
A new topology for sub multilevel inverter has been evolved and a generalized MLI brought out from a series connection of sub multilevel inverter. Efforts have been paid to obtain optimal structure regarding different criteria such as the number of switches, starting voltage on the switches and number of dc voltage sources [13]. A variable frequency carrier band PWM (VFCBPWM) method has been outlined for firing the switches in the cascaded MLI and espouses the ability to generate different output voltage levels [14]. The simulation results have been projected to establish the lowering of harmonics at lower switching frequencies and the consequent reduction in the THD levels.

The trend revolves around the use of reduced switched count configurations that perceive paths for the flow of current from a smaller number of power sources and still allow achieving the desired number of levels.

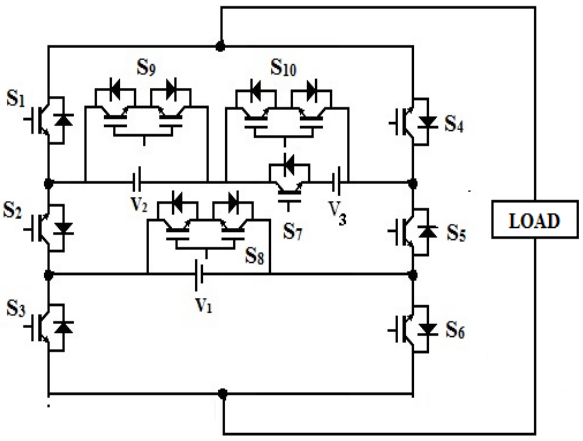
The primary effort orients to examine the use of a variable frequency carrier band (VFCB) modulating mechanism for producing a variable multilevel voltage from a single phase proposed MLI. The theory entices the implementation of VFCBPWM algorithm through the FPGA portal in order that it serves to lower the THD of the output voltage and current of the single phase proposed MLI. The procedure envisages experimentally testing the performance of the MLI over a range of operating loads.

2. POWER MODULE

The Fig.1 (a) shows the generalized power circuit for the proposed topology formed with dc power sources, unidirectional and bidirectional switches. The structure of the MLI includes a facility to add as many sections, with two unidirectional and a bidirectional switch together with a voltage source in each section for producing the desired number of levels of the output voltage. The connection diagram seen in Fig. 1(b) enables to extract a seven level output from the MLI and the schematic in Fig. 2 explains the modes of operation to generate $+3V_{dc}$ and $-3V_{dc}$ for the output voltage. The entries in Table 1 relate to the switches involved in each mode of operation of the MLI.



(a)

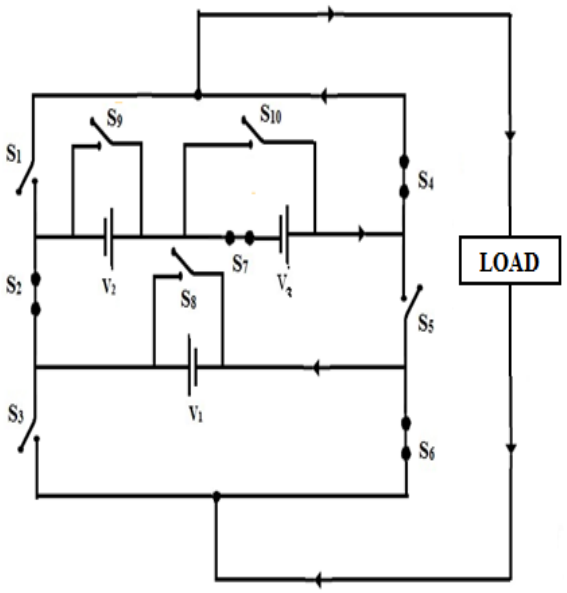


(b)

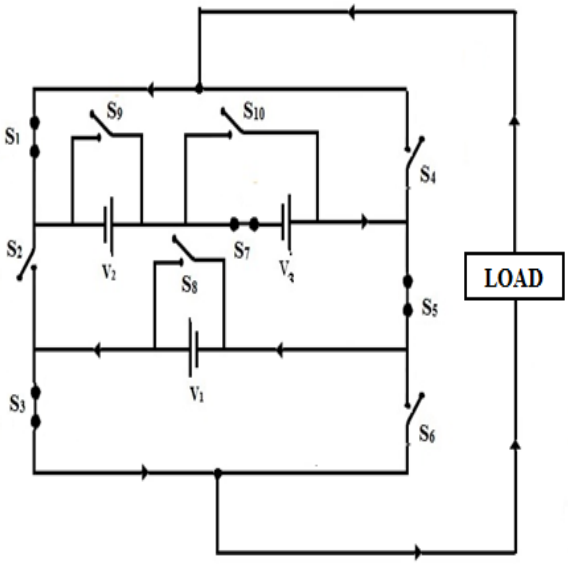
Fig.1 (a) Generalized structure of the proposed single phase MLI **(b)** Proposed MLI topology for seven-level output

The entries in Table 2 compare the number of main switches, bypass diodes, clamping diodes, dc split capacitors, clamping capacitors and dc sources among similar other topologies. The line graph in Fig. 3 draws out a comparison of the number of power switches required for obtaining higher levels of output voltage with that of the cascaded H-bridge multilevel inverter (CHBMLI).

It shows that the number of power devices increases in the order 3n+1 for the proposed MLI and 4n for the CHBMLI, where n represents the number of dc voltage sources in the circuit, as the level of the output voltage increases. It clearly depicts the reduction in switch count of the new MLI over varying levels of the output voltage.



(a)



(b)

Fig.2 (a) Mode of operation for +3Vdc output
(b) Mode of operation for -3Vdc output.

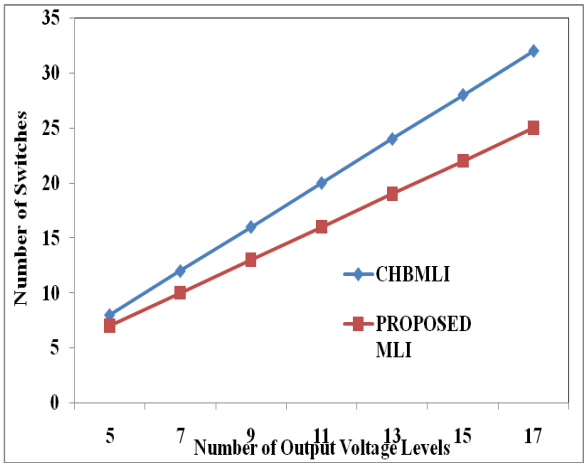


Fig.3 Comparison of proposed MLI and CHBMLI.

Table 1 Conduction Sequence for seven level output

Output Voltage Levels	Conduction of Switches									
	S_1	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**	**S_9**	**S_{10}**
$+V_{dc}$	√	√				√				
$+2V_{dc}$		√		√		√				√
$+3V_{dc}$		√		√		√	√			
$0V_{dc}$	√	√	√							
$-V_{dc}$			√	√	√					
$-2V_{dc}$	√				√	√	√			
$-3V_{dc}$	√		√		√		√			

Table 2 Comparison between proposed and conventional topologies for 'm' level

Multilevel inverter structure	Cascaded H-bridge	Diode clamped (1981)	Flying Capacitor	Multilevel dc-link inverter			Proposed
				Cascaded half bridge	Diode Clamped	Flying capacitor	
Main switches	2(m-1)	2(m-1)	2(m-1)	(m-1)+4	(m-1)+4	(m-1)+4	(3m-1)/2
Bypass diodes	-	-	-	-	-	-	-
Clamping diodes	-	2(m-3)	-	-	(m-3)	-	-
DC split capacitors	-	(m-1)/2	(m-1)/2	-	(m-1)/2	(m-1)/2	-
Clamping capacitors	-	-	(2m-6)/2	-	-	(2m-6)/4	-
DC sources	(m-1)/2	1	1	(m-1)/2	1	1	(m-1)/2

3. MODULATION STRATEGY

The PWM signals echo to be pulse trains with fixed frequency and magnitude and enjoy a variable pulse width. The width of the pulses changes in accordance with the design of the modulating signal [15-17]. The frequency of a PWM signal must be higher than that of the modulating signal such that the energy delivered to the load depends mostly on the modulating signal.

The simplest way to generate a PWM signal results from the intersection method, which requires only a triangular waveform and a reference sinusoidal signal. In spite of the existence of a numerous methods, the traditional sinusoidal pulse width modulation (SPWM) technique fosters to be a prominent choice for generating the switching pulses for the MLI. However the drawbacks in SPWM technique such as pulse dropping and mode changing the lower output voltage with higher THD level necessitate looking for alternatives [18-20].

Owing to the reason that the fixed frequency carrier based PWM affects the switch utilization in MLIs, the variable frequency Carrier band (VFCB) PWM which uses the conventional sinusoidal reference signal and the carrier signals with variable frequency comes in to be handy [21]. The pulses appear when the amplitude of the modulating signal goes beyond that of the carrier signal.

The number of switching per modulation cycle (t) in each level of the inverter depends on the carrier frequency for that level and the duration of time across which the reference waveform dwells within the level's corresponding time band. If the carrier frequency for all the levels remains identical, the top and bottom levels may experience a higher switching than the intermediate levels.

The scheme enables the variation of the carrier frequency of each band based on the time duration for which the reference waveform dwells in the carrier band with a purpose to balance the switching action. The band crossing times, where the reference waveform crosses from one band to adjacent band can be computed using the amplitude symmetry of the sine wave about the time axis. The band dwell times in radians (starting at the band adjacent to zero axis) is determined from Eqn. 1

$$t_{band_n} = 2\left(t_{n+1} - t_n\right) \tag{1}$$

$$\text{where} n = 0,1,2,3,.....,\left[\frac{m-1}{2}\right] \tag{2}$$

Owing to the symmetry of the sine wave about the zero axis, the bands below the zero axis can be related as in Eqn. 3

$$tband_{-n} = tband_n \tag{3}$$

The relation between the number of switching per bands, N_{sw_n}, and the frequency ratio m_{f_n}, for each band n of an inverter can be expressed as in Eqn.4

$$m_{f_n} = \frac{\pi.N_{sw_n}}{tband_n} = \frac{\pi.N_{sw_n}}{2\left(t_{n+1} - t_n\right)} \tag{4}$$

The frequency ratio for each band allows to be set in order that each level in the inverter contains approximately the same number of active device switching per cycle for all the levels. The hybrid frequency is deduced from the above equations to compute the variable frequencies for the carrier signals.

Among the different options that revolve around the phase disposition (PD), alternative phase opposition disposition (APOD) and carrier polarity variation (CPV) varieties, the

PD based approach pulls in a higher preference because it compares the carrier signals of the same frequency, amplitude and phase with a dc offset that lie in different levels within a single sine modulating signal [22].

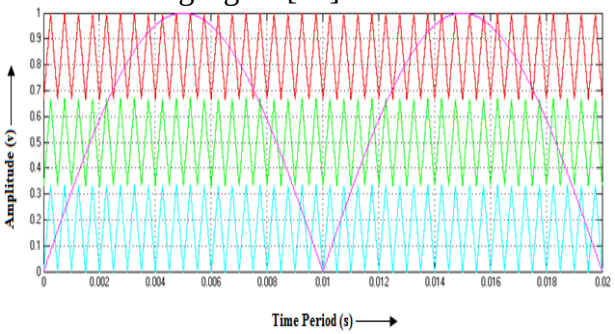


Fig.4 Reference and Carrier arrangement for PD MCPWM

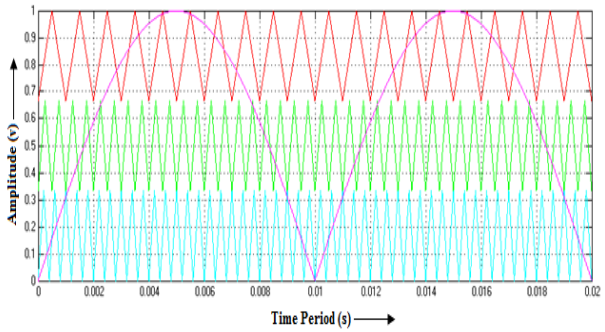


Fig. 5 Reference and Carrier arrangement for PD VFCBPWM

The Figs. 4 and 5 depict the process of alignment of the reference and the carrier wave using the PD theory for both MCPWM and the VFCBPWM through which it derives the pulses for the switches in the MLI

4. SIMULATION RESULTS

The efforts orient an investigative study of the VFCBPWM scheme for operating a seven level proposed MLI with RL load of 100 ohms and 150 mH respectively with the three dc sources in the MLI each of 100 volts in magnitude. The Figs. 6 to 11 compare the output voltage waveform along with their respective THD spectra and load current waveform for the PD based MCPWM and VFCBPWM at the same operating load and a modulation index of 1.

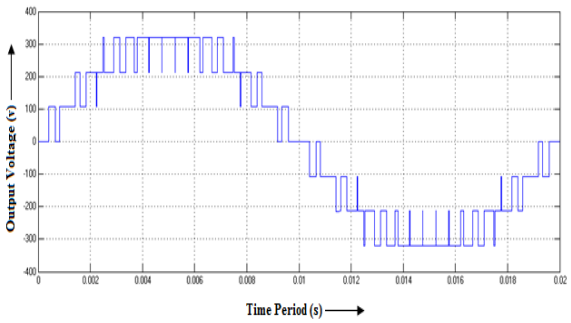


Fig.6 Output voltage waveform for PD MCPWM

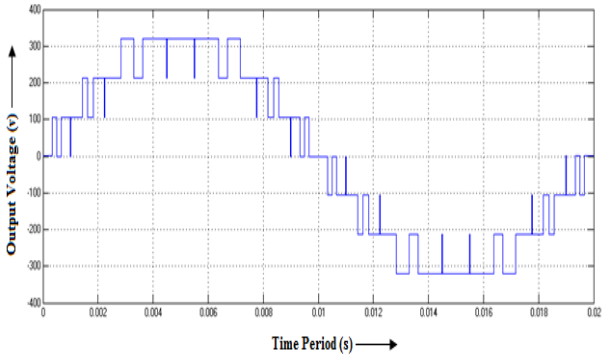


Fig.7 Output voltage waveform for PD VFCBPWM

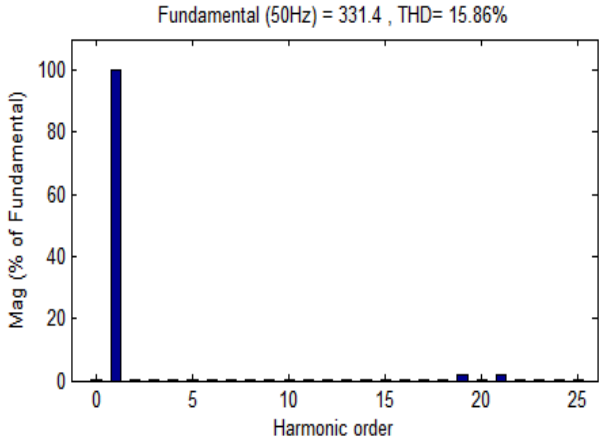


Fig.8 Output voltage spectrum for PD MCPWM

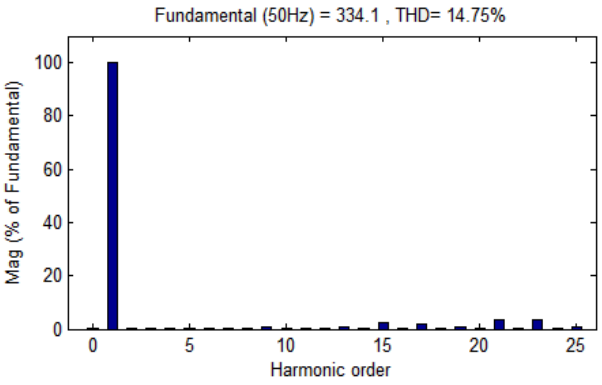


Fig.9 Output voltage spectrum for PD VFCBPWM

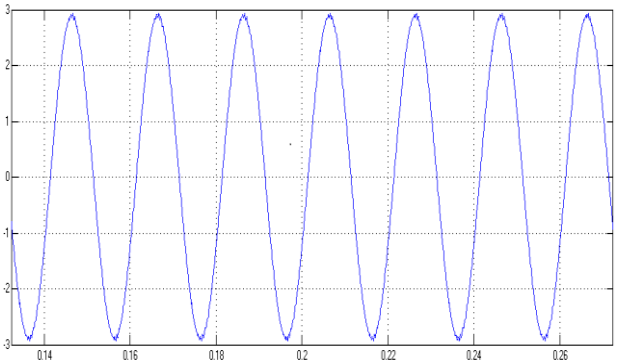


Fig.10 Output current waveform for PD MCPWM

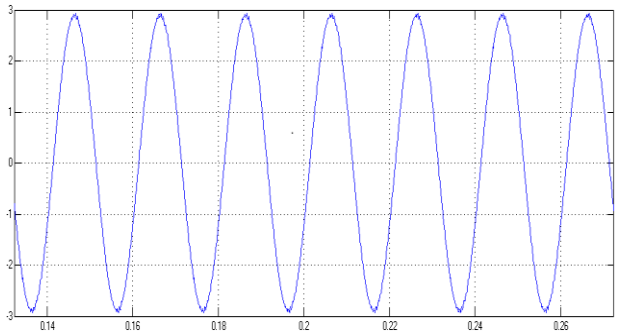


Fig.11 Output current waveform for PD VFCBPWM

The bar and line diagrams drawn in Figs.12 and 13 for the output phase voltage and its corresponding THD respectively obtained for the operating range of modulation indices shows that the VFCBPWM imbibes the ability to mitigate the multiple frequency components of the output voltage and extracts a higher output voltage and a lower THD than the MCPWM.

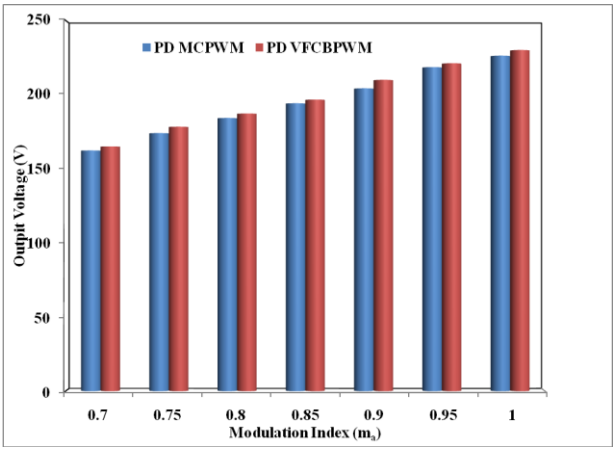


Fig.12 Modulation index Vs Phase voltage

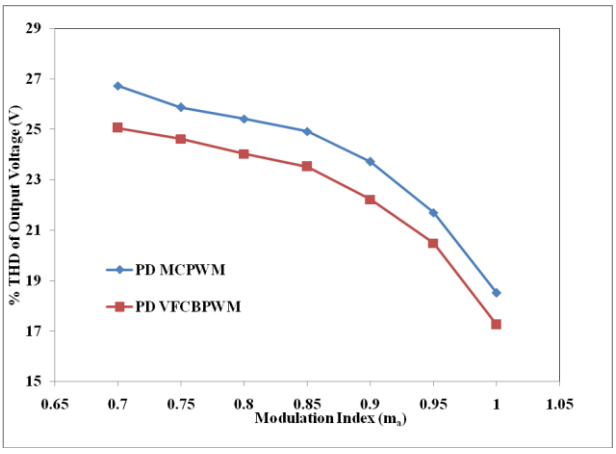


Fig.13 Modulation index Vs Phase voltage

5. HARDWARE IMPLEMENTATION

The study owes to construct a prototype of the MLI seen in Fig. 14 using unipolar (*IRG4BC20UPBF)* and bipolar (FIO 50-12BD) insulated gate bipolar transistor (IGBT) of ratings similar to those used in simulation. The associated gate driver circuits and the field-programmable gate array (FPGA) used for generating the PWM pulses seen in Fig. 15 form part of the experimental arrangement.

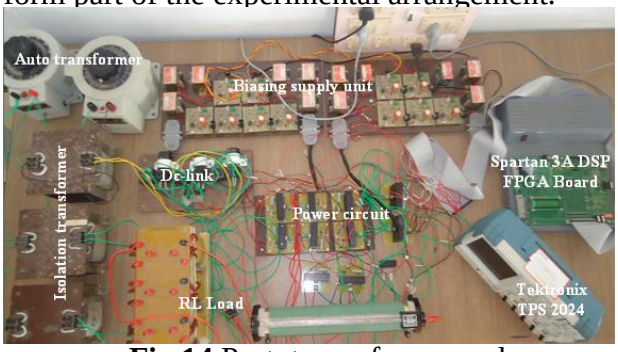


Fig.14 Prototype of proposed seven level MLI

Fig.15 Gating pulses

The FPGA consists of an integrated circuit designed to be configured by a customer or a designer after manufacturing hence field-programmable. The configuration interleaves a generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC).

It contains an array of programmable logic blocks and a hierarchy of reconfigurable interconnects that allow the blocks to be wired together like many logic gates that can be inter-wired in different configurations. The logic

blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND & XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory. It endows an ability to enable easy, fast and flexible implementation of the controller circuit in the hardware.

The prototype seeks the role of Xilinx based system generator facility available as a toolbox in MATLAB to generate the VFCBPWM pulses for the power switches in the MLI. The scheme involves an VHDL code appropriate mechanism for the VFCBPWM strategy through which the Xilinx Spartan XC3SD1800A-FG676-4 Spartan 3A DSP FPGA board buffers to turn on the power switches in the MLI. The Figs .16 and 17 depicts the output voltage along with their corresponding THD spectra for the VFCBPWM formulations respectively.

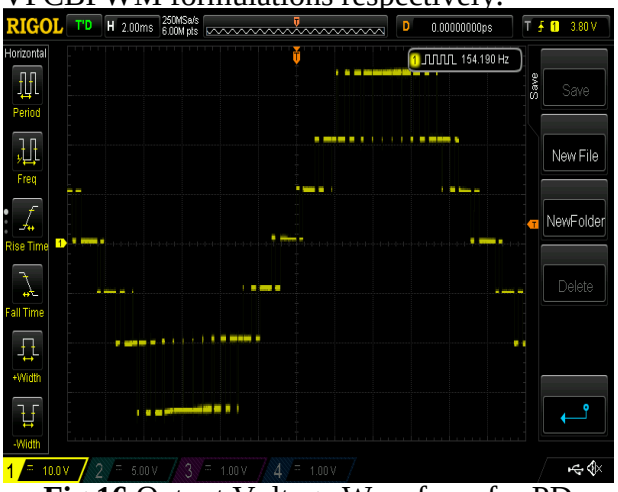


Fig.16 Output Voltage Waveform for PD VFCBPWM

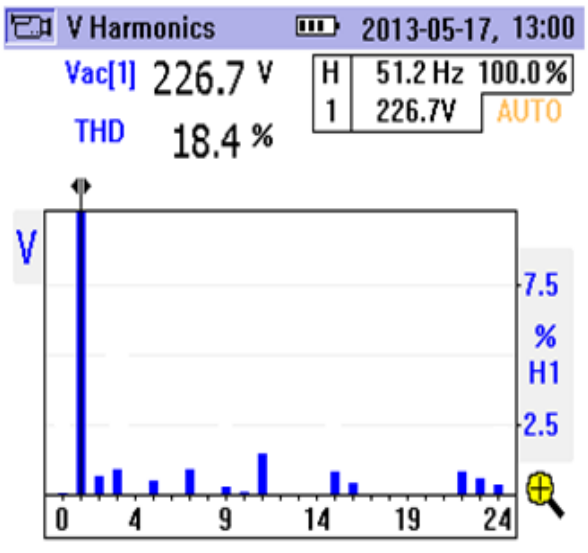


Fig.17 Output voltage spectrum for PD VFCBPWM

Table 3 Comparison of simulation and experimental results using VFCBPWM

Target Fundamental Output Voltage (V)	%THD for output voltage	
	SIM	HW
100	25.01	25.52
120	24.33	25.54
140	23.62	24.82
160	22.56	23.55
180	20.51	21.17
200	19.11	20.73
220	17.97	18.62

The entries in Table 3 serve to adequately validate the simulated and hardware results through a close comparison of the output voltage over a range of specified targets. The fact that the methodology produces the same fundamental output for the projected output level both using simulation and hardware with comparable THD values goes to validate the VFCBPWM technique in addition to highlighting the practical feasibility of the new MLI configuration. The fact that the output voltage magnitude increases along with a decrease in THD decreases serves to bring out that the new structure eclipses a lower harmonic content of the output voltage for a projected target.

6. CONCLUSION

A new single phase MLI has been developed with a perspective to reduce the number of switches in the path for the flow of current. The variable frequency carrier band PWM technique has been realized to generate seven level output voltage. The methodology has been articulated to effectively modify the modulation index range over the operating range and arrive at the desired target voltage. The VFCBPWM technique has been able to provide full utilization without any pulse dropping and mode changing. The results reveal the ability of the modulation strategy to reduce the harmonic content and facilitate a lower THD along with an increase in the fundamental component. The experimental results have been portrayed to validate the simulated performance and showcase a new dimension for the role of this PWM approach. The new topology has been a revelation of the ability of the MLI to synthesize the ac output

voltage and bestow it to suit the emerging needs of the industrial world.

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