NOVEL SUPER LIFT LUO-CONVERTER BASED ON SHEPPARD-TAYLOR TOPOLOGY

[1]A. Deepa, [2]Dr.K. Sathish Kumar

[1]School of Electrical Engineering, VIT University, Tamil Nadu, India, E-mail: deepame2k@gmail.com
Corresponding author. Tel: +91-988056588.

[2]Associate Professor, School of Electrical Engineering, VIT University, Tamil Nadu, India, E-mail: kansathh21@yahoo.co.in, Tel: +91-9443623508

Abstract: *This article presents a novel negative output elementary super lift Luo converter (NOESLLC) based on the Sheppard-Taylor (S-T) topology operated in a continuous inductor current with the classical proportional-integral (PI) controller for high voltage applications. The NOESLLC based on S-T is one of the topologies of DC choppers. The advantages of NOESLLC based on S-T over the traditional NOESLLCs are reduced ripples in the inductor current and capacitor voltage, high output voltage generation with minimum duty ratio, high voltage transfer gain, and a simpler structure. The NOESLLC based on S-T is built with fewer components and devices compared to the S-T converter and the conventional NOESLLC. Further, it is capable of manipulating the output voltage and produces good efficiencies at different operating stages through different input voltages, load resistances, and duty cycles. The importance of NOESLLC based on S-T over the traditional soft switching converters is that its main switches close with Zero Current Switching (ZCS) and the diodes open with Zero Voltage Switching (ZVS). In this study, the classic PI controller was designed for NOESLLC on the basis of S-T to improve its dynamic performance and output voltage regulation for different supply voltages and load resistance variations. The characteristics of the NOESLLC based on S-T using a classical PI controller are verified through a MATLAB/Simulink model under different working conditions compared with the traditional NOESLLC. The results show that the NOESLLC based on S-T is more capable in comparison with the conventional NOESLLC.*

Keyword: *Super lift Luo-converter, negative output super lift Luo-Converter, sheppard taylor, continuous conduction mode, soft-switching, zero transition switching, classical PI controller and state-space average modeling.*

NOMENCLATURE

V_{in}	Input voltage
C_1, C_2 and C_3	Energy storage Capacitors
L	Inductor
V_L	Voltage across the inductor
D_1, D_2, D_3, D_4	Diodes
V_{c1}	Voltage across the capacitor one
V_o	Output voltage
d, d_1	Duty ratio
T	Switching time period
V_{c3}	Voltage across the capacitor 3
L_B	Critical inductance
i_L	Inductor current
i_o	Output current
V_{c2}	Voltage across the capacitor 2
I_{in}	Input current
P_o	Output power
P_{in}	Input power
i_{LB}	Inductor current at boundary
R	Load resistance
R_B	Boundary load resistance
T_B	Switching time period at boundary
S_1 and S_2	Switches

I. INTRODUCTION

Recently, the switching mode power supplies and regulators have been used extensively over the traditional linear power supplies as they have good efficiency, are compact and light weight, cost effective and work on smaller power ratings (about 28 W). In recent times, DC-DC converters have played a major role in commercial applications such as mobile phones, medical equipment, computer hardware parts, robot systems, LED TVs, and military applications [1].

The Sheppard-Taylor (S-T) converter is commonly used to generate non-pulsating input/output currents analogous to the C´uk converter [2]. The S-T topology is examined as a possible development topology of the C´uk topology. The direction of power flow in a C'uk converter circuit is bi-directional, whereas the S-T topology circuit operates uni-directionally.

The S-T converter consists of dual storage coils that can shape the input current and feed the output load thereby reducing the input and output current ripples. It is capable of regulating the output voltage while the input voltage and load resistance are modified. The S-T converter can regulate the output voltage more efficiently due to an insensitive input resistance compared to the C´uk converter. Therefore, it is better suited for power factor correction (PFC) applications [3]. In general, the S-T converter structure consists of 4 diodes and 2 power switches working in synchronization. Further, the lack of synchronization between the 2 switches does not lead to converter break down. A drawback of the S-T converter is the nominal ON/OFF power loss particularly when the converter operates at higher frequencies.

A lot of investigations on PFC applications based on the S-T converter have been reported in the surveys [4-10]. Yet, not a large amount of improvement on S-T topology has been reported [7-9]. The new boost DC-DC converters based on the S-T has been reported [11]. The key merits of boost converter based on S-T are capable of regulating the output voltage during a wide range of input voltage or load variations, constructed with fewer components compared with the normal S-T converter topology. Main switches of this converter are closed with Zero-Current-Switching (ZCS), and the rectifier diodes are open with Zero-Voltage-Switching (ZVS). The negligible input current ripple of this converter makes the input filter not essential and works at lower duty ratio.

Considerable work has been done on the applications of PFC based on the S-T converter [4-10]; however, there are not many studies available on the improvements of S-T topology [7-9]. Studies on the new boost DC-DC converters based on S-T are well accomplished [11] with key merits being the capability of manipulating the output voltage in input voltage and load resistance variations and having fewer components compared with the traditional S-T converter topology. In this converter, Zero-Current-Switching (ZCS) is achieved by turning on the main switches whereas the Zero-Voltage-Switching (ZVS) is obtained by turning off the diodes. The converter does not require an input filter due to a small amount of input current ripple and works on lower duty ratio.

Luo converters (LCs) belong to a new class of DC-DC converters which originate from the basic DC-DC converters employing voltage lift techniques (VLT) [12]. The merits of LCs over the traditional DC-DC converters are excellent voltage transfer gain, increased power density, good efficiency, output capacitor voltage, and inductor current with lesser ripples, economical topology, simple structure, and getting rid of parasitic elements [13-15]. The negative output elementary super lift Luo converter (NOESLLC) [16] is one of the topologies of LCs. In this article, the NOESLLC is considered for S-T study with classical Proportional-Integral (PI) controller. The PI controller for double output elementary Luo converter was presented in [17]. The output voltage response of the converter with designed PI controller produces more peak overshoots, about 15V, for the line and load disturbances.

A series of negative output VLT-C'uk converters have been developed [18]. The step-up DC-DC converter with the coupled inductor and VLT was studied [19]. However, it creates good voltage transfer gain with a complex structure The general modeling and design of the Sliding Mode Controller (SMC) for triple lift LC using Super Lift Technique (SLT) have been well accomplished [20]. The ZVS-QR based elementary circuit of VLT and SLT converters using an analog controller UC 3861 was proposed earlier [21-22]. However, with this controller, the efficiency of these converters came to be 91%.

The classical PI controller for positive output super lift converter with PV system has been studied [23]. Its start-up region has been found to produce maximum overshoots of around 16V. The modeling and simulation of KY voltage boost converter with a direct method of sliding mode controller (SMC) were carried out [24]. This design control method produced peak overshoots of 4V and 1V respectively for in line and load variations. A complete study of the negative output KY boost converter with the classical linear proportional-integral (PI) controller was carried out [25], and huge overshoots and longer settling times were reported. The SMC with the intelligent controller for positive output elementary split inductor type boost converter has been studied [26]. Until now, this controller has produced good characteristics during various stages. The SMC along with proportional dual integral controller for negative output super lift converters have been studied [27-30]. The design

controlled technique for these converters produced more peak overshoot and ripples in the capacitor voltage.

From the available literature, it is clear that NOESLLC based on S-T has not been studied so far. Hence in this article, a NOESLLC based on S-T operated in CCM using a classical PI controller has been proposed. The state space equations of this converter were derived and the classical PI controller parameters were determined. The performance of NOESLLC based on S-T using PI controller was validated under different operating conditions via a MATLAB/Simulink model compared to the traditional NOESLLC.

II. THE CONSTRUCTION AND ANALYSIS OF NOESLLC BASED ON S-T

The NOESLLC based on S-T is shown in Fig. 1 (a). It consists of two power switches (S_1 and S_2), four diodes (D_1, D_2, D_3, D_4), one inductor L, three capacitors (C_1, C_2, C_3), an input voltage V_{in}, and a load resistance R. The inductor current is kept constant at all times by choosing large values for L, C_2, and C_3. The operation of NOESLLC based on S-T consists of three modes, illustrated in Fig. 1.

In Mode 1 (see Fig. 1b), S_1 and S_2 are closed, C_1 is de-energized, D_1, D_2, and D_4 are open and D_3 is closed. The inductor current rises linearly as ($V_{in} + V_{c1}$). The input source and C_1 dispense energy to L. At the beginning of Mode 1, the voltage of C_1 is ($V_{in} - V_L$), thus the energy in C_1 is $C_1 (V_{in} - V_L)^2/2$.

In Mode 2 (see Fig. 1c), S_1 and S_2 are open, D_3 is closed and D_4 is open while V_{c1} is less than V_o, C_1 is energized to help the source and the inductor through D_1 and D_2, and the inductor current i_L falls.

In Mode 3 (see Fig. 1d), while V_{c1} is more than V_o, D_4 conducts since V_{c1} is less than the V_o. The input supply and inductor provide power to the load R.

The analysis of the designed converter (Fig. 1a) was performed by making the following assumptions:

- The NOESLLC based on S-T works in a constant state,
- The current in the coil is continuous,
- The capacitor size is large and a constant voltage V_o is maintained,
- The switches are ON for a period dT and OFF for period (1-dT)
- The circuit elements are ideal.

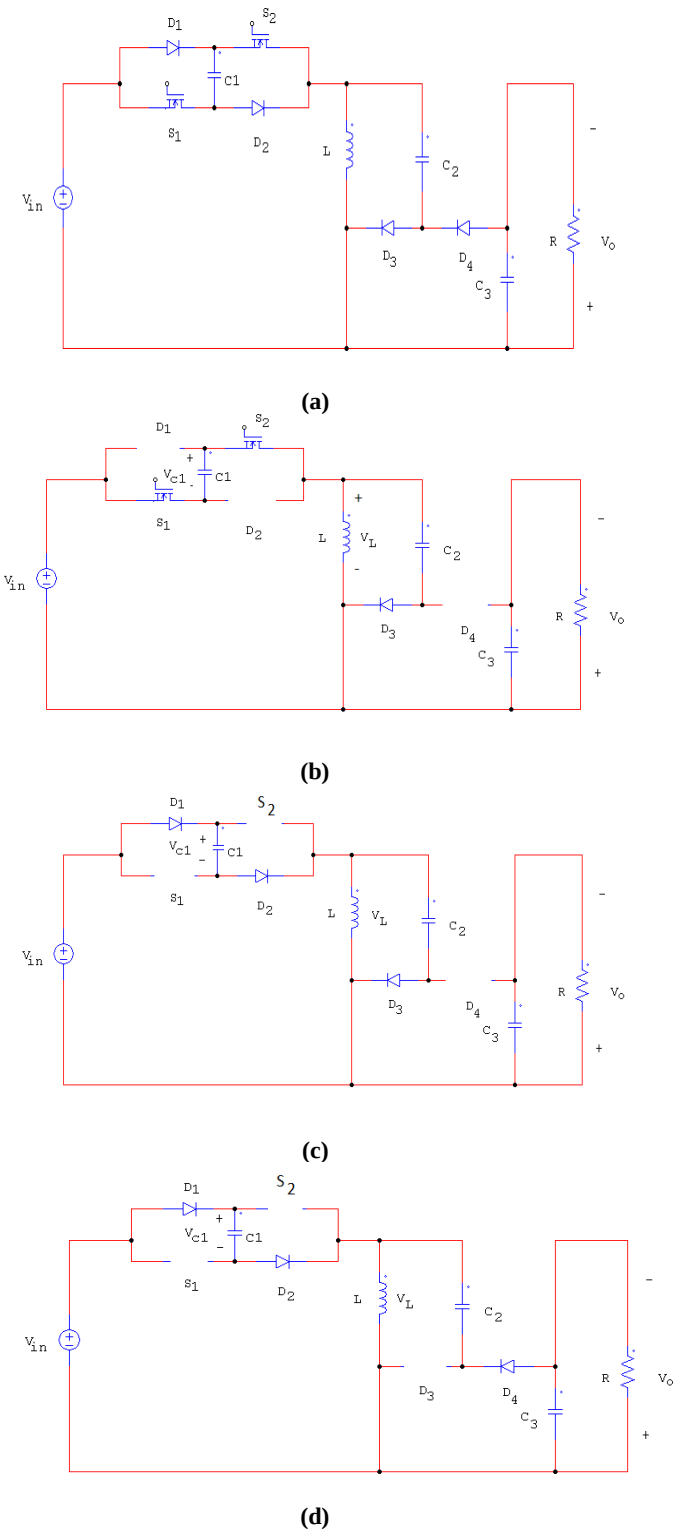


Fig.1. The NOESLLC based on S-T, (a). Topology, (b). Mode 1 operation, (c). Mode 2 operation and (d). Mode 3 operation.

A. Mode 1 Operation Analysis

In Mode 1 (Fig. 1b), S_1 and S_2 are closed and V_L is derived from the Kirchhoff's Voltage Law (KVL).

$$\begin{aligned} V_L &= V_{in} + V_{c1} \\ \frac{di_L}{dt} &= \frac{V_{in} + V_{c1}}{L} \\ V_{c3} &= V_o \end{aligned} \tag{1}$$

While di_L/dt is a positive constant, the current rises linearly and is expressed as

$$(\Delta i_L)_{closed} = \left(\frac{V_{in} + V_{c1}}{L} \right) dT \tag{2}$$

B. Mode 2 Operation Analysis

In Mode 2 (refer the Fig. 1c), the switches S_1 and S_2 are open, and the D_4 is open, since $V_{c1} < V_o$. The C_1 is charged by the source and the inductor. The voltage across the inductor V_L is expressed as (3)

$$\begin{aligned} V_L &= V_{in} - V_{c1} \\ \frac{di_L}{dt} &= \frac{V_{in} - V_{c1}}{L} \\ V_{c3} &= V_o \end{aligned} \tag{3}$$

While, the di_L/dt is a negative constant, the current is fall linearly as shown in Fig. 1c and it is written as (4)

$$(\Delta i_L)_{open} = \left(\frac{V_{in} - V_{c1}}{L} \right)(1 - dT) \tag{4}$$

For steady-state working, the i_L at the end of the T is the same as that at the start, which means that the net change in i_L over one complete period is null

$$(\Delta i_L)_{Closed} + (\Delta i_L)_{Open} = 0 \tag{5}$$

Substituting (2) and (4) in (5) becomes

$$\begin{aligned} (V_{in} + V_{c1})dT + (V_{in} - V_{c1})(1 - dT) &= 0 \\ V_{c1} &= \frac{V_{in}}{1\text{-}2d} \end{aligned} \tag{6}$$

C. Mode 3 Operation Analysis

In Mode 3 (see Fig. 1d), S_1 and S_2 are open and D_4 is closed. Prior to Mode 3, the V_{c3} reduces due to freewheeling. At the end of Mode 2 ($t=d_1T$), C_1 continues to be energized, the diode D_4 conducts when $V_{c1}=V_o$ and V_{c1} is clamped at V_o, (the corresponding circuit is shown in Fig. 1d). At $t=d_1T$, $V_{c1}=V_{c3}=V_o$ and the capacitor voltages are specified by

At (t=dT)

$$\begin{aligned} V_{c1}(dT) &= \frac{-1}{C_1} \int_0^{dT} i_L dt + V_{c1}(dT) \\ V_{c1}(dT) &= \frac{-1}{C_1} i_L dT + V_{c1}(0) \end{aligned} \tag{7}$$

at $t=d_1T$,

$$\begin{aligned} V_{c1}(d_1T) &= \frac{1}{C_1} \int_{dT}^{d_1T} i_L dt + V_{c1}(dT) \\ V_{c1}(d_1T) &= \frac{1}{C_1} i_L (d_1\text{-}d)T + V_{c1}(dT) \end{aligned} \tag{8}$$

Substituting (7) into (8)

$$\begin{aligned} V_{c1}(d_1T) &= \frac{1}{C_1} i_L (d_1\text{-}d)T - \frac{1}{C_1} i_L dT + V_{c1}(0) \\ V_{c1}(d_1T) &= \frac{1}{C_1} i_L (d_1\text{-}2d)T + V_{c1}(0) \end{aligned} \tag{9}$$

Similarly,

$$\begin{aligned} V_{c3}(d_1T) &= \frac{-1}{C_3} \int_0^{d_1T} i_o dt + V_{c3}(0) \\ V_{c3}(d_1T) &= \frac{-1}{C_3} i_o d_1 T + V_{c3}(0) \end{aligned} \tag{10}$$

Let, $V_1 = V_{c3}$, we solve for d_1

$$\frac{1}{C_1} i_L (d_1\text{-}2d)T + V_{c1}(0) = \frac{-1}{C_3} i_o d_1 T + V_{c3}(0)$$

$$\frac{1}{C_1} i_L (d_1\text{-}2d)T = \frac{-1}{C_3} i_o d_1 T$$

(11)

By applying the power balance condition and it is expressed as (12)

$$P_{in} = P_o = V_{in} i_L = V_0 i_0$$

(12)

Simplifying the (12) and then

$$i_0 = (1\text{-}2d) i_L \quad (13)$$

Substituting (13) into (11)

$$\frac{1}{C_1} i_L (d_1\text{-}2d)T = \frac{-1}{C_3} (1\text{-}2d) i_L d_1 T$$

$$d_1 = \frac{2C_3 d}{C_3 + C_1(1\text{-}2d)} \quad V_o = V_{c1} = \frac{V_{in}}{1\text{-}2d}$$

(14)

D. Critical Inductance Analysis

The critical inductance L_B (B indicates the boundary) is bounded between the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM). The average value of the inductor current at the boundary $i_{LB,}$ is

$$i_{LB} = \frac{1}{2} \Delta i_L$$

(15)

Owing to

$$\Delta i_L = \frac{V_{in} + V_{c1}}{L} dT = \frac{V_{in} - V_{c1}}{L} (1\text{-}d)T$$

(16)

Substituting (16) into (15)

$$i_{LB} = \frac{V_{in} + V_{c1}}{2L} dT = \frac{(1\text{-}2d)V_{c1} - V_{c1}}{2L} dT$$

$$= \frac{V_o}{L} (1\text{-}d) dT$$

(17)

Therefore, if the average output current is smaller than i_{LB}, given by (17), then i_L will become discontinuous.

$$i_{oB} = i_{LB}(1\text{-}2d) = \frac{V_o T}{L} d(1\text{-}d)(1\text{-}2d)$$

$$i_o \succ i_{oB} = \frac{V_o T}{L} d(1\text{-}d)(1\text{-}2d)$$

(18)

From (18), the required L to ensure a CCM of the NOESLLC based on S-T is

$$L \succ L_B = \frac{V_o T}{I_{oB}} d(1\text{-}d)(1\text{-}2d)$$

$$= d(1\text{-}d)(1\text{-}2d)RT \quad (19)$$

$$R \succ R_B = \frac{V_o}{I_{oB}} = \frac{L}{d(1\text{-}d)(1\text{-}2d)T}$$

(20)

$$T \succ T_B = \frac{L}{d(1\text{-}d)(1\text{-}2d)R}$$

(21)

E. Output Ripple Voltage Analysis

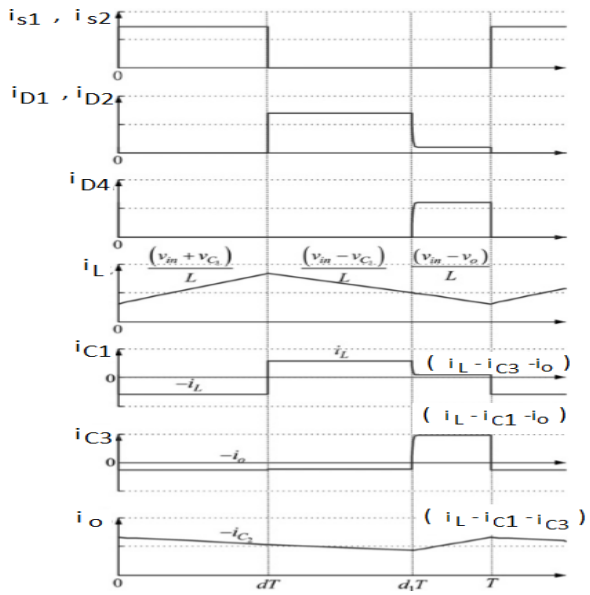
The above-deduced equations are derived with the assumption that V_o is kept fixed. In real-time executions, instabilities in V_o or the voltage ripples always exist. The ΔV_o can be evaluated from the capacitor current as indicated in Fig. 2. The ΔQ is expressed as (22).

$$|\Delta Q| = \frac{V_o}{R} d_1 T$$

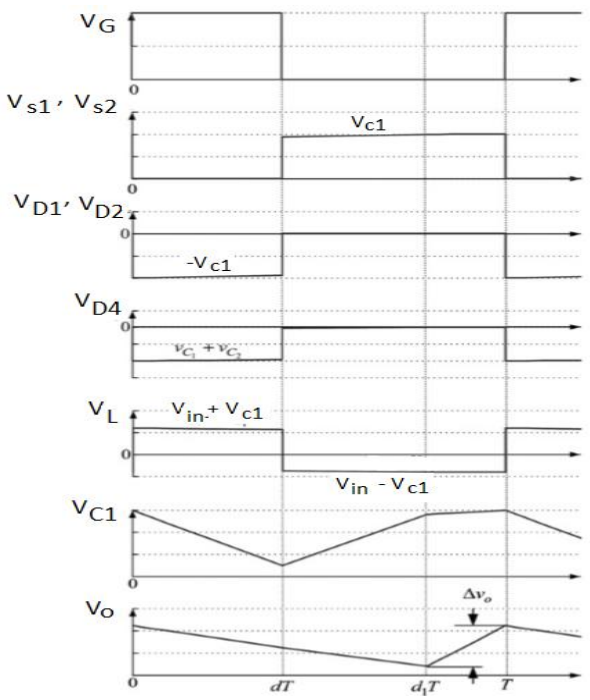
(22)

An expression for output ripple voltage is

$$\Delta V_o = \frac{\Delta Q}{C_3} = \frac{I_o}{C_3} d_1 T = \frac{V_o}{RC_3} d_1 T \quad (23)$$



(a)



(b)

Fig.2 Theoretical waveforms in time period of T, (a) voltages and (b) currents.

III. STATE SPACE AVERAGED MODELING OF NOESLLC BASED ON S-T

A. Modeling of NOESLLC based on S-T

The state space equations for Fig. 1 (b) can be expressed as (24) and for Fig. 1 (d) can be written as (25).

$$\begin{cases} \dot{i}_L = \dfrac{V_{in}}{L} \\ \dot{V}o = -\dfrac{V_o}{C_3 R} \end{cases} \quad \text{Switch closed (24)}$$

$$\begin{cases} \dot{i}_L = \dfrac{V_{in} - V_o}{L} \\ \dot{V}o = \dfrac{i_L}{C_3} - \dfrac{V_o}{C_3 R} \end{cases} \quad \text{Switch open (25)}$$

Using the charge balance rule on C_1, Eq. (26) for T can be written. Here k denotes the status of the switch (d=1 when the switch is closed and d=0 when it is open).

$$dC_2 \frac{dV_{C2}}{dt} + (1-d) i_L = 0 \quad (26)$$

As there are two capacitors in NOESLLC, with $V_{C2} = V_{in}$, V_o alone can be chosen as a state space variable (not V_{in}). Similarly, with the inductor current i_{L1}, entire space variables of the NOESLLC based on S-T can be chosen as i_L, V_o, x_1, and x_2. From (24), (25), and (26), the modeling of NOESLLC based on S-T in CCM may be written and is given by (27).

By (24), (25), and (26), the modeling of the NOESLLC based on S-T in CCM may be written by (27)

$$\begin{bmatrix} \dot{i}_L \\ \dot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1-d}{L} \\ \dfrac{1-d}{C_3} & -\dfrac{1}{RC_3} \end{bmatrix} \begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} V_{in} \quad (27)$$

B. Design of classical PI controller

A classical PI controller (shown in Fig. 3) is chosen for providing good output voltage regulation and reduced steady state errors for NOESLLC based on S-T. The dc output voltage is measured and compared with suitable reference output voltage that produces the voltage error

signal. This error signal is applied to the PI controller to produce the control signal. This control signal is compared with carrier triangular signal to generate the Pulse Width Modulation (PWM) pulses for switches in NOESLLC based on S-T to keep the output voltage stable and minimize the steady state errors. The classical PI controller parameters, proportional gain (K_p) and integral times (T_i), are obtained with the help of Zeigler-Nichols tuning method. From this method, the NOESLLC based on S-T provides a sustained oscillation with ultimate gain (K_{cr} = 0.00025) and ultimate period (P_{cr} = 0.0012 s) resulting in the parameter values as $K_p = K_{cr}/2$=0.00012 and $T_i = P_{cr}$ /1.2=0.001 s [27].

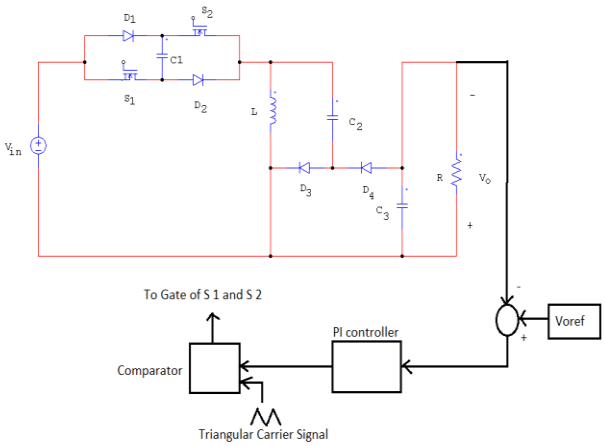
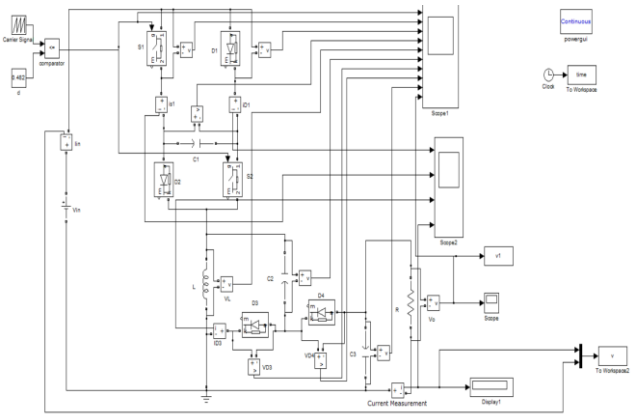


Fig. 3. The figure shows NOESLLC based on S-T with a classical PI controller.

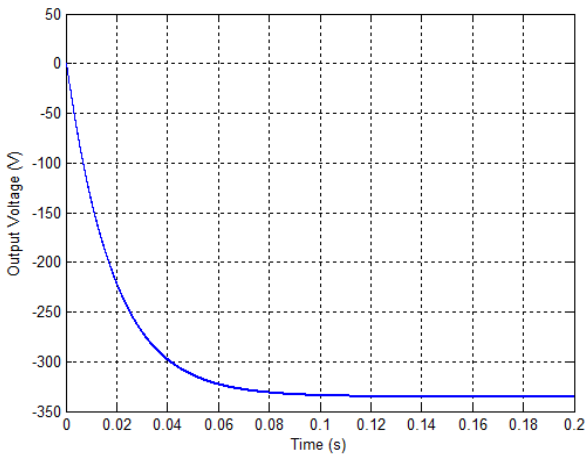
IV. SIMULATION RESULTS

Table 1. The table lists specifications of NOESLLC based on S-T.

Parameters name	Symbol	Value
input voltage	V_{in}	12V
output voltage	V_o	-333.33V
Inductor	L	50μF
Capacitors	C1,C3,C2	25μH,60 μH, 200μH
nominal switching frequency	f_s	100KHz
load resistance	R	50Ω
average output current	I_o	-6.8A
duty ratio	D	0.482
peak to peak capacitor ripple	ΔVo	-0.1V



(a)



(b)

Fig. 4. The figure shows (a) MATLAB/Simulink model of the NOESLLC based on S-T and (b) simulated output voltage responses of the NOESLLC based on S-T.

This section deals with the simulation results of NOESLLC based on S-T topology with and without a controller in different operating regions as compared to the conventional NOESLLC. The specifications of the designed converter are given in Table 1. Figure 4(a) shows the MATLAB/Simulink model of the designed converter and Fig. 4(b) shows the simulated output voltage responses of the designed converter. The figure clearly shows that the output voltage of the NOESLLC based on S-T could produce −333.3V, which matches well with the theoretical value (see Table 1). Figure 5 shows the simulated voltage responses of the NOESLLC based on S-T. From these results, one can infer (a) the gate voltage of the switches V_G, (b) voltage across: (i) the capacitor V_{c1}, (ii) the diodes V_{D1} and V_{D2}, (iii) the switches V_{s1} and V_{s2}, (iv) the diodes V_{D3} and V_{D4}, (v) the capacitors V_{c3} and V_{c4}, and (c) the output voltage V_o. The results match very closely with the theoretical results (see Fig. 2). It is also

found that the diodes are open with ZVS (marked as circles in Fig. 4).

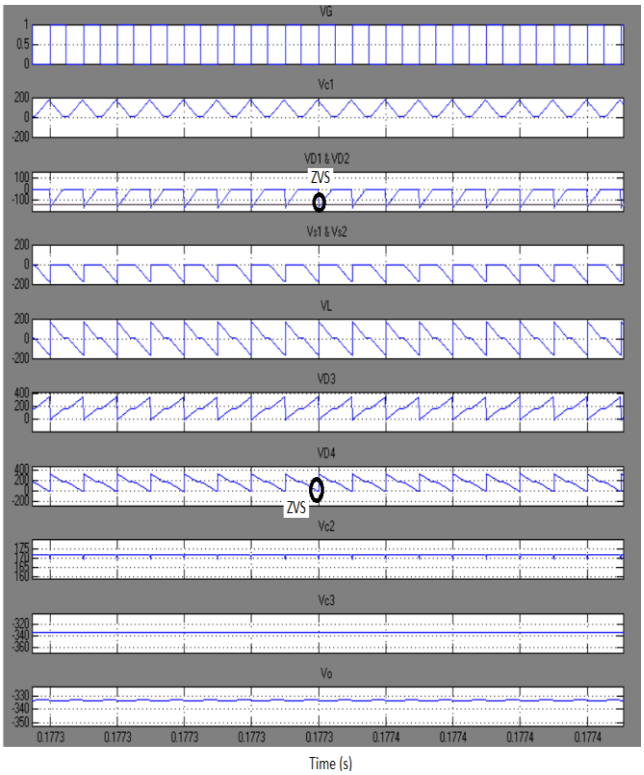


Fig. 5. The figure displays simulated voltage responses of the NOESLLC based on S-T.

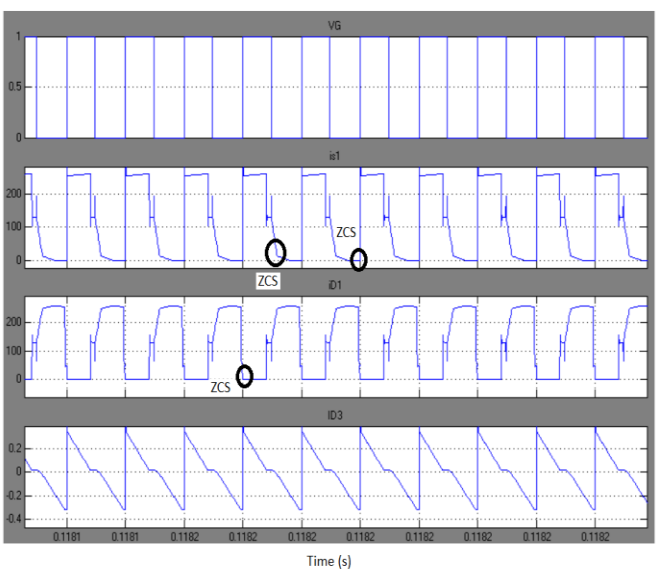


Fig. 6. The figure shows simulated current responses of the NOESLLC based on S-T.

Figure 6 shows the simulated current waveforms of the NOESLLC based on S-T. These waveforms give the gate voltage of switches V_G, current through the switch I_{s1} and current through the diodes. It is found that the switches are closed with ZCS (marked as circles in Fig. 5) and the results match closely with the theoretical results (see Table 1). Figure 7 shows the output and input current of the NOESLLC based on S-T which clearly shows that the simulated values of the same converter are matching the theoretical values (refer Table.1). Figure 8 shows the simulated output voltage and the input voltage responses of the designed converter using a classical PI controller for step change input voltage varied in the range from 12V to 15V and from 15V to 12V at time = 0.14 s. It is found that the output voltage of the NOESLLC based on S-T produced negligible overshoot and faster settling time.

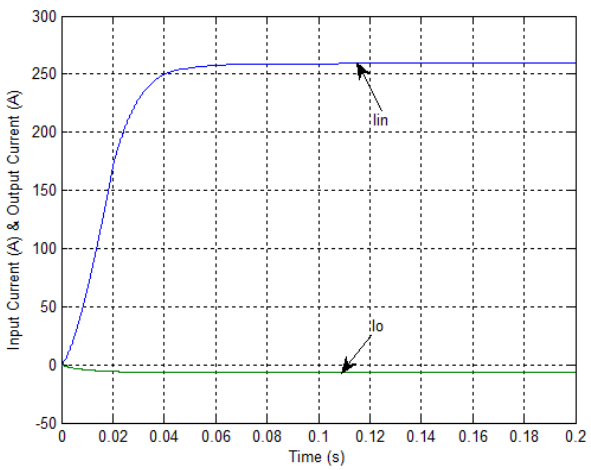


Fig. 7. Simulated output and input current responses of the NOESLLC based on S-T are shown in the figure.

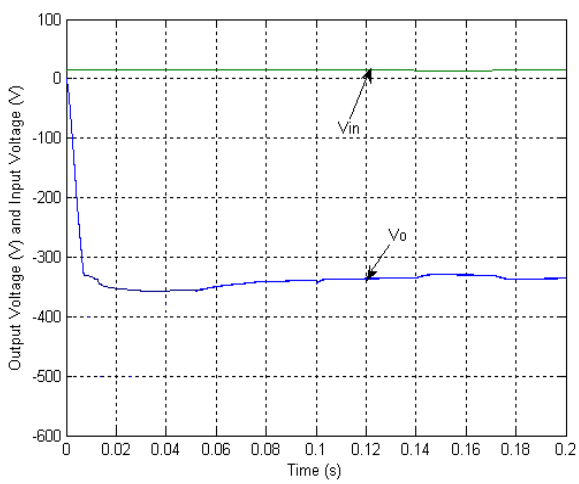


Fig. 8. Simulated output and input voltage responses of the NOESLLC based on S-T using a classical PI controller with an input voltage variation from 12V to 15V and 15V to 12V are displayed.

CONVENTIONAL NOESLLC:

Figure 9 shows MATLAB/Simulink model of the conventional NOESLLC. The output voltage and current through the switch of the conventional NOESLLC are shown in Fig. 10 and Fig. 11. The output voltage of the *conventional NOESLLC converter produced* $V_o = -36V$ *for* $V_{in} = 12V$, $R = 50$ *ohm*, $f_s = 100kHz$ and d = 0.482. The current through the switch gets more distorted (shown in Fig. 11) because of hard switching. Hence, the efficiency of this converter gets affected due to increased switching losses which cause EMI. Figure 12 shows the simulated output voltage and input voltage responses of the NOESLLC using a PI controller when the input voltage is varied from 12V to 15V and 15V to 12V. It is found that the output voltage of the NOESLLC using controller produced maximum overshoots of -26V and a settling time of 0.015 s.

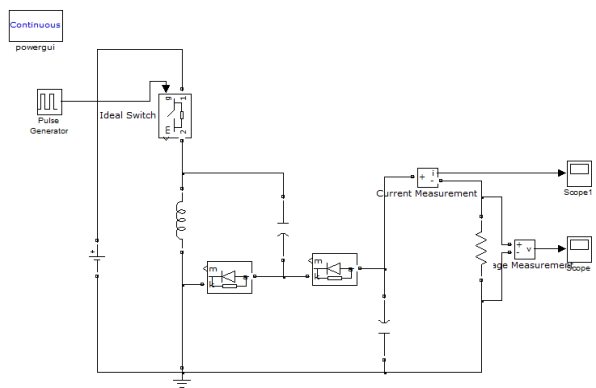


Fig. 9. The MATLAB/Simulink model of a traditional NOESLLC.

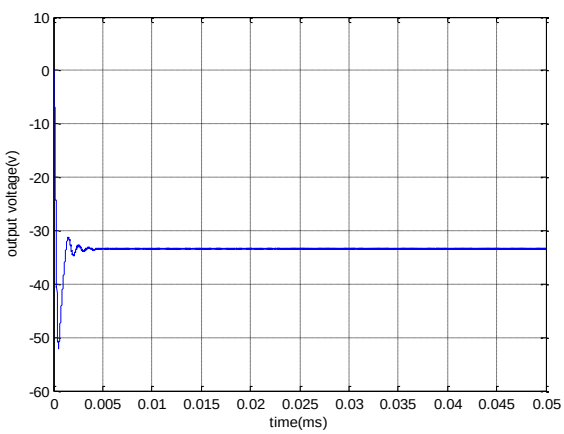


Fig. 10. The simulated output voltage response of the traditional NOESLLC.

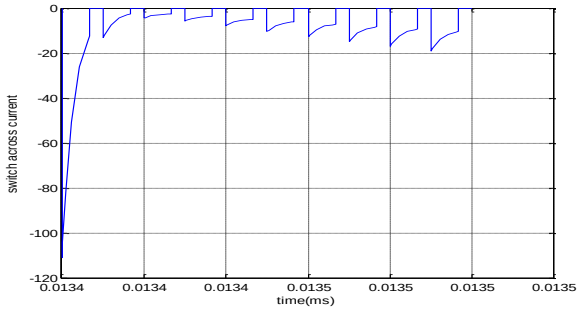


Fig. 11. Current through the switch of a traditional NOESLLC.

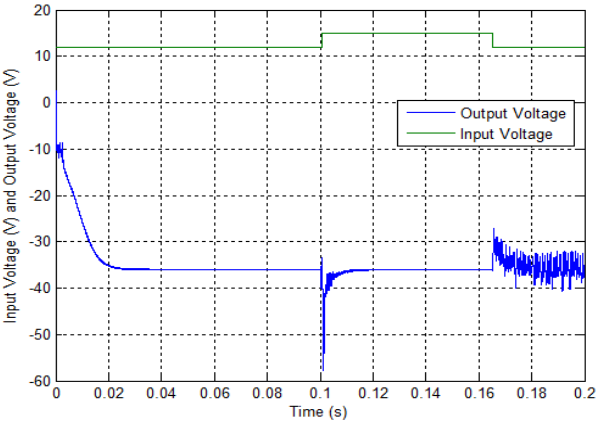


Fig. 12. Simulated output voltage response of the traditional NOESLLC using a PI controller is shown.

Time domain analysis and different input voltage variations of the NOESLLC based on S-T with and without controller are cataloged in Tables 2, 3 and 4. From these tables, it is clear that the designed converter performs well in the different working states.

Table 2. The summarizes the performance of the NOESLLC based on S-T for various input voltage.

V_{in} (V)	V_o (V)	I_o (A)	P_o (W)	Output Ripple voltage
12	-333.3	-6.6	2199.78	-0.0036
14	-388.8	-7.776	3023.3	-0.01227
16	-444.4	-8.88	3946.272	-0.0139
18	-500	-10	5000	-0.0182
20	-555.5	-11.11	6160.5	-0.019

Table 3. Time Domain Analysis of the NOESLLC based on S-T using Controllers in Transient Region

NOESLLC based on S-T	With PI controller	Without controller
Results	**Simulation**	**Simulation**
Rise time(s)	0.01	0.02
Settling time(s)	0.06	0.12
Peak overshoot (%)	-2	0
Steady state error	0	0
Output Ripple Voltage(V)	-0.0012	-0.0032

Table 4. Time domain Analysis of the NOESLLC based on S-T using Controllers over the conventional NOESLLC

Results	**NOESLLC based on S-T**	**Transient Region**		**Line variations From 12V to 15V and 15V to 12V**		**Load variations From 50 ohm to 60 ohm and 50 ohm to 40 ohm**	
		Maximum Overshoots (V)	**Settling Time (s)**	**Maximum Overshoots (V)**	**Settling Time (s)**	**Maximum Overshoots (V)**	**Settling Time (s)**
Simulation	**NOESLLC based on S-T** With PI controller	-2	0.06	-1	0.012	-1	0.012
	NOESLLC with PI controller	-16	0.005	-26	0.015	-24	0.015

V. CONCLUSIONS

The design, analysis, operation and output voltage regulation of the new NOESLLC based on S-T with the classical PI controller has been shown through the MATLAB/Simulink software platform. Soft switching analysis of the NOESLLC based on S-T was performed, which can lead to fewer switching losses. The NOESLLC based on S-T was found to produce good efficiency, a high output voltage with minimum duty ratio, and fewer ripples in the capacitor voltage and inductor current in comparison with the traditional NOESLLC. The results reported here prove the proficiency of NOESLLC based on S-T with different input/output voltage and duty cycle operating conditions in comparison with the traditional NOESLLC. In addition, the NOESLLC based on S-T with the classical PI controller was found to produce good dynamic performance in line and load variations, superior output voltage regulation and fine time domain specification analysis over the traditional NOESLLC. Therefore, it was found to be more suitable for high voltage applications. Further, a non-linear controller is also being developed for the NOESLLC based on S-T to improve its performance and experimental model is under construction.

REFERENCES

1. Cuk, S., Middlebrook, R.D., *"Advances in switched-mode power conversion part I*," IEEE Trans. Indust. Electron., 1983, IE-30, pp. 10–19.
2. Ismail, E.H., Sabzali, A.J., Al-Saffar, M.A., *"A high-quality rectifier based on Sheppard–Taylor converter operating in discontinuous capacitor voltage mode,"* IEEE Trans. Indust. Electron., 2008, 55,pp. 38–48.

3. Tse, C.K., Chow, M.H.L.*,"Single stage high power factor converter using the Sheppard–Taylor topology,"* 27th Annual IEEE Power Electronics Specialists Conf. (PESC), 1996, pp. 1191–1197.
4. Tse, C.K., Chow, M.H.L., *"New single-stage PFC regulator using the Sheppard–Taylor topology,"* IEEE Trans. Power Electron., 1998, 13,pp. 842–851.
5. Rezanezhad, M., Dargahi, M., Lesan, S., Noee, A.R., *"Sliding mode control of modified Sheppard–Taylor PFC converter*," IEEE Int. Multitopic Conf. (INMIC), 2008, pp. 38–41.
6. Rezanejad, M., Dargahi, M., Lesan, S., Noee, A.R., Karami, M.,Joshani, M., *"Study and control of Sheppard–Taylor DC–DC converter*," IEEE Second Power and Energy Conf. (PECon), 2008,pp. 219–223.
7. Rezanejad, M., Dargahi, M., Lesan, S., Noee, A.R., Karami, M., *"New switching method for Sheppard–Taylor PFC converter,"* IEEE Second Int. Power and Energy Conf. (PECon), 2008, pp. 793–796.
8. Liang, Z., Bo, Z., Huasheng, M., Xuechao, L., *"Research and experiment of Sheppard–Taylor topology,"* Proc. 31st Annual Conf. of IEEE Industrial Electronics Society (IECON), 2005, pp. 1235–1240.
9. Kanaan, H.Y., Hayek, A., Al-Haddad, K., *"Multi-loops control design for a new Sheppard–Taylor based Factor Corrector with model-nonlinearity compensation,"* IEEE Int. Symp. on Industrial Electronics (ISIE), 2008, pp. 105–110.
10. Kanaan, H.Y., Hayek, A., Al-Haddad, K., *"A new single-phase power factor corrector based on the sepic and Sheppard–Taylor topologies,"* Proc. 29th Int. Telecommunications Energy Conf. (INTELEC), 2007, pp. 840–847.
11. Chih-Chiang Hua, Hsi-Chin Chiang, Chih-Wei Chuang, *"New boost converter based on Sheppard-Taylor topology,"* IET Power Electronics, Vol.7, Iss. 1, January 2014, p. 167 – 176.
12. Fang Lin Luo, *"Luo-Converters, a series of new DC-DC step-up (boost) conversion circuits,"* Proceedings of IEEE Conference on Power Electronics and Drive Systems - 1997 (PEDS'97), Singapore, May 1997, pp. 882-888.
13. Fang Lin Luo, *"Luo-Converters: voltage lift technique,"* Proceedings of IEEE Power Electronics Special Conference (PESC'98), Fukuoka, Japan, May 1998, pp. 1783-1789.
14. Fang Lin Luo, Hong Ye, and Muhammad H. Rashid, *"Multiple-lift push-pull switched-capacitor Luo-Converters,"* Proceedings of IEEE Power Electronics Special Conference (PESC'02), Cairns, Australia, June 2002, pp. 415-420.
15. Fang Lin Luo and Hong Ye, *"Negative output multiple-lift push-pull SC Luo-Converters,"* Proceedings of IEEE Power Electronics Special Conference (PESC'03), Acapulco, Mexico, June 15-19, 2003, pp. 1571-1576.
16. Fang Lin Luo and Hong Ye, *"Negative output super-lift converters,"* IEEE Transactions on Power Electronics, Vol.18, No.5, September 2003, pp. 1113-1121.
17. A. Joseph Basanth, S.P. Natrajan, and T.S. Sivakumaran, *"Simulation and DSP based implementation of conventional controller for double output elementary Luo-Converter,"* Proceedings of 3rd International Conference on Power Electronics Systems and Applications (PESA'09), May 2009, pp. 1-6.
18. M. Zhu and F.L. Luo, *"Voltage-lift-type Cuk converters: topology and analysis,"* IET Power Electronics, Vol.2, No.2, 2009, pp. 178–191.
19. S.K. Changchien T.J. Liang, J.F. Chen, and L.S. Yang, *"Step-up dc-dc converter by coupled inductor and voltage-lift technique,"* IET Power Electronics, Vol.3, No.3, 2010, pp. 369–378.
20. Y. Jiao, F.L. Luo, and M. Zhu, *"Generalised modeling and sliding mode control for n-cell cascade super lift dc-dc converters,"* IET Power Electronics, Vol.4, No.5, 2011, pp. 532–540.
21. E. Jayashree and G. Uma, *"Design and implementation of zero-voltage switching quasi-resonant positive output Luo converter using analog resonant controller UC3861*," IET Power Electronics, Vol.4 No.1, January 2011, pp. 81–88.
22. E. Jayashree and G. Uma, *"Analysis, Design and implementation of zero-voltage switching quasi-resonant positive output super lift Luo-converter,"* IET Power Electronics, Vol.4 No.1, January 2011, pp. 21–28.
23. Zeng-Li Shan Shuo Liu and Fang-Lin Luo, *"Investigation of a super-lift Luo-Converter used in solar panel system,"*Proceeding of China International Conference on Electricity Distribution (CICED'12), Shanghai, September 2012, pp.1-4.
24. S.Sentamil Selvan, K.Ramash Kumar, R.Bensraj, *"Modeling, Simulation and Design of Variable Structure Based Sliding Mode Controller for KY-Voltage Boosting Converter,"* Wseas Transactions On Circuits And Systems, Vol. 15, 2016, pp.143-154.
25. S.Senthamil Selvan, R.Bensraj, K.Ramash Kumar, N.P.Subramaniam, *"Design, Analysis, Simulation Study and Corroboration of Classical Controller for a Negative Output KY Boost Converter,"* International Journal of Applied Engineering Research, Vol. 10 No.51, 2015, pp. 485-494.
26. K.Ramash Kumar, S.Jeevananthan, S.Ramamurthy, *"Improved Performance of the Positive Output Elementary Split Inductor-Type Boost Converter using Sliding Mode Controller plus Fuzzy Logic Controller,"* Wseas Transactions On Systems And Control, Vol. 9, 2014, pp. 215-228.
27. K. Ramash Kumar, *"Implementation of sliding mode controller plus proporotinal double integral controller for neagtive output elementary boost converter,"* Alexandria Engineering Journal, (Elsevier), Vol. 55, No. 2, 2016, pp. 1429-1445.
28. R. Kalaivani, K. Ramash Kumar, S. Jeevananthan, *"Implementation of VSBSMC plus PDIC for Fundamental Positive Output Super Lift-Luo Converter,"* Journal of Electrical Engineering, Vol. 16, Edition: 4, 2016, pp. 243-258.
29. N.Arunkumar, T.S.Sivakumaran, K. Ramash Kumar, *"Improved Performance of Linear Quadratic Regulator plus Fuzzy Logic Controller for Positive Output Super Lift Luo-Converter,"* Journal of Electrical Engineering, Vol. 16, Edition:3, 2016, pp. 397-408.
30. Ramash Kumar, K., Jeevananthan, S., *"Design of sliding mode control for negative output elementary super lift Luo-Converter operated in continuous*

conduction mode," ICCCCT'10, Tamilnadu, India, pp. 138-148.